NI PXI-5404

- 1 channel updated at 300 MS/s
- 9 kHz to 105 MHz sine wave
- DC to 100 MHz clock
- 1.07 µHz frequency resolution
- 1 to 4 V_{pp} sine amplitude
- 12-bit vertical resolution
 ±0.2 dB flatness of sine wave
- passband (9 kHz to 100 MHz)
- Ideal for coherent sampling
 applications
- Phase-lock loop for synchronization to other devices and PXI backplane

Operating Systems

• Windows 2000/NT/XP/Me/9x

Recommended Software

- LabVIEW
- LabWindows/CVI

Other Compatible Software

- Visual Basic
 C/C++
- C/C++

Driver Software (included)

NI-FGEN

Calibration Certificate Included



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pxi5404

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Overview

The National Instruments PXI-5404 is a 100 MHz frequency generator packaged in 1-slot PXI module. It generates sine and clock outputs simultaneously at up to 100 MHz with 1.07 μ Hz resolution. By using direct digital synthesis (DDS) and precise phase-lock loop circuitry, the PXI-5404 generates stable, accurate sine and clock outputs of which you can programmatically adjust the amplitude, frequency, and phase of the sine and clock outputs as well as the duty cycle of the clock output.

The PXI-5404 is a versatile, cost-effective, sine wave generator with output levels ranging from 1 to 2 $_{Vpp}$ into a 50 Ω load with 12-bit resolution, excellent frequency resolution, and passband flatness. Stimulus-response instruments such as network analyzers and ATE test systems will benefit from using the PXI-5404 as the sine stimulus because of its passband flatness, and its frequency accuracy and resolution.

The PXI-5404 can also serve as a programmable clock generator for ATE systems because of its 1.07 μ Hz frequency resolution, dutycycle adjustability from 25 to 75 percent, and programmable voltage levels of 5, 3.3, or 1.8 V into high-impedance loads.

Ideal for Coherent Clocking Applications

With the simultaneous sine and clock outputs, you can employ coherent clocking to reduce the test time of your device under test (DUT) and eliminate the need for antialias filtering. Because you have a precise phase and frequency relationship between the

analog stimulus and the sample clock, there is no need for windowweighting functions in your FFTs for spectral analysis, thus reducing the need to sample the DUT over several cycles of the sine stimulus. With a coherent clocking system, you know both the analog stimulus and the sampling clock frequencies, thus eliminating the need for antialias filters or time-domain window functions. In a coherent sampling system, all the power from the signal and its accompanying harmonics fall into predictable frequency bins.



Figure 1. A typical coherent sampling application is the testing of analog-to-digital converters (ADCs). Here the sine stimulus is fed to the ADC and the clock output is phase locked and multiplied to yield a sampling clock to the ADC and to a digital pattern generator/analyzer.



Programmable Clock Output Levels for TTL/CMOS

The PXI-5404 has programmable voltage output levels of 5, 3.3, and 1.8 V into high impedance loads and 2.5, 1.65, and 0.9 V into a 50 Ω load. With the flexible clock output levels, the PXI-5404 can address both TTL and CMOS technologies thereby making it an attractive clock source for ATE systems. Additionally an external DC blocking capacitor can be used to shift the outputs to other popular logic levels such as LVPECL and PECL.

Superior Leveled Sine Output Accuracy

The PXI-5404 employs an onboard amplitude-leveling compensation scheme whereby the specified output level enjoys excellent accuracy of ± 0.2 dB within the passband of 9 kHz to 100 MHz. In Figures 2 and 3 the effects of the output leveling technique can be seen clearly. This level accuracy makes the PXI-5404 an ideal source for many applications such as communications and ATE, where amplitude accuracy is a key requirement.



Figure 2. NI PXI-5404 Passband Flatness without Onboard Compensation

Phase-Lock Loop for Synchronization

The phase-lock loop on the PXI-5404 synchronizes sine and clock generation to an external clock. The reference clock source may come from the front panel connector CLK IN, the PXI 10 MHz reference clock on the PXI backplane, or the PXI trigger bus. The PXI-5404 phase-locks to frequencies from 3 to 20 MHz in 1 MHz increments. The PXI-5404 can also operate without an external reference frequency by using its onboard frequency source.

Using phase-lock loops, you can synchronize two or more PXI-5404 sources to within 0.022 deg in phase for outputs up to 100 MHz. Consequently, you can build a high-performance multichannel source on the PXI platform. Thus, with the PXI-5404 you can address applications such as in automotive and video test that require multiple clock frequencies that are phase locked in precise phase relationships.



Figure 3. NI PXI-5404 Passband Flatness with Onboard Compensation

Triggering

The sine and clock outputs can run continuously or you can use triggering controls to start sine and clock generation. Trigger sources can be either external or internal (software trigger). External triggers can be received from the front panel connector PFI0, the PXI trigger bus, or the PXI star trigger bus. You can also change the operating frequency, amplitude, and phase of the PXI-5404 output from one of these sources.

Calibration

Every PXI-5404 is factory calibrated and shipped with a calibration certificate verifying that it meets NIST-traceable standards. Periodically, you can externally calibrate the PXI-5404 (provided you have the expertise and equipment), or you can ship it to National Instruments or a qualified metrology lab. External calibration is usually performed on an annual basis. Visit **ni.com/calibration** for more information about calibration services.

I/O Connector

The PXI-5404 has five SMB connectors labeled SINE, CLOCK, REF IN, REF OUT, and PFI0. The sine and clock outputs are accessed on SINE and CLOCK, respectively, and an external reference frequency for the phase-lock loop is fed to the REF IN connector. The REF OUT connector is a truly versatile output connector that can route out a signal from multiple sources, including the onboard VCXO reference (divided by 1 to 255), the star trigger bus, the PXI trigger bus, PFI0 connector, and the PXI 10 MHz reference clock. The PFI0 connector is a bidirectional connector. As an input, the PFI0 connector can accept a trigger that initiates sine and clock generation from an external source. As an output, the PFI0 connector.

Software

If you want to build an automated test application or integrate the PXI-5404 in your test software, use the IVI-compliant NI-FGEN instrument driver with:

- NI LabVIEW
- •NI LabWindows/CVI
- Microsoft Visual Basic
- •Microsoft Visual C/C++

NI-FGEN comes with a comprehensive set of examples that illustrate the programming and features of the PXI-5404 in all four programming environments. Because NI-FGEN offers simulation mode, you can run your application on a laptop PC, for example. Thanks to this feature, you can develop your application with the PXI-5404 remotely or a team of developers can work on an application without the need for hardware in their systems.

Interactive Control

The PXI-5404 comes with the versatile Sources Soft Front Panel with which you can interactively control the PXI-5404. You can generate sine and clock outputs with control of frequency, phase, amplitude, and duty cycle with the Sources Soft Front Panel. Furthermore, you can run the PXI-5404 in simulation mode from the Sources Soft Front Panel.

Ordering Information

NI PXI-5404778577-01

Includes the module, NI-FGEN, Sources Soft Front Panel, and calibration certificate.

Specifications a Temperature Ra	ande unless othe	perating rwuse noted		Connector	Channel U Clo	ock Uutpu		
Outer of Cha		-		Frequency Ba	anae			
Output Una	aracteristic	S		Frequency Re	esolution			
Number of outp	outs	1	sine and 1 clock,	Phase Range				
		Bo	oth generate same frequency	Phase Resolu	ition			
		si	multaneously.	Output Impe	dance			
CHO SINE (Cha	nnel O Sine Wav	e Output, I/O	Panel Connector)	Output Prote	ction			
Connector		SI	MB					
Frequency Rang	ge		kHz to 105 MHz	Output	5.0 V Level	3.3 V Lev		
Frequency Reso	olution	1.	07 μHz	Current	120 mA	72 mA		
Phase Range		0	to 359.978 deg	Amplitude	5.0 V Level	3.3 V Lev		
Phase Resolution	on	16	5384 steps including endpoints	(Open Load)	Min Max	Min N		
		(a	pproximately 0.022 deg)	Vol	-0.10 V 0.40 V	-0.10 V 0.4		
Output Impeda	nce		0 Ω ±4% (9 kHz to 105 MHz)	VOH	4.00 V 5.30 V	2.60 V 3.7		
Output Protecti	on) V _{rms}	Amplitude	5.0 V Level	3.3 V Lev		
Sampling Rate.			00 MS/s	(50 Load)	Min Max	Min N		
Amplitude Rand	ae			Vol	-0.10 V 0.20 V	-0.10 V 0.2		
Open load		4.	00 _{Vpp} to 2.00 _{Vpp}	И	2.00 V 2.65 V	1.30 V 1.8		
50 Ω load		2.	00 ypp to 1.00 ypp	- 011				
Amplitude Reso	olution		048 steps including endpoints	Rise/Fall Time				
		(C	Den Load: Approximately 977 uV.	Duty Cycle Range				
		50	$\Omega \mid \text{oad: Approximately 489 µV}$	Duty Cycle A	ccuracv			
Amplitude Accu	iracy	+	1% @ 50 kHz	30	to 70%			
Amplitude Pass	band Flatness	+(0.2 dB relative to the amplitude @	25	and 75%			
) kHz 9 kHz < f < 105 MHz					
Amplitude Tem	nerature Coefficie	ent +(0.013% / 40	PFI 0 (Progra	mmable Fund	tion Inter		
Vertical Resolut	ion	12	2 hits @ 4 V (open load)	Connector				
vortical ricsolat			L bits @ 2 V., (open load)	Direction				
Bandwitdth		10	15 MHz (0.2 dB)	Frequency Range				
Filtor		Δ.	nalog 7-nole elliptical	As an Input				
1 11(01				Destination for	or Input Signal			
SINAD	1 MHz	+ 51 dB	Amplitude set to 1.8 v_{ee} (~ -1 dBFS)	1				
5110.0	10 MHz	+ 48 dB	Measured from 9 kHz to 150 MHz					
	20 MHz	+ 45 dR						
	50 MH-	+ 45 UD	1	Input Resista	nce			
		± 42 UD ⊥ /12 dD	1	Input Protect	ion			
	1 MU~	+ 42 UD	Amplitudo 1.9., (1.dPES)	VIH				
SEDB		- JJ UDU	Manufulue 1.0 Vpp (~ -1 uBFS).	Vii				
SFDR	I I U IVIMZ	- 04 UDC	Interview Interview	Output Prote	ction			
SFDR	20 MIL	40 JD.		Suparriote				
SFDR	20 MHz	- 49 dBc	includes narmonics.					
SFDR	20 MHz 50 MHz	- 49 dBc - 45 dBc	includes narmonics.					
SFDR	20 MHz 50 MHz 100 MHz	- 49 dBc - 45 dBc - 53 dBc		-				
SFDR	20 MHz 50 MHz 100 MHz 1 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB	Amplitude 1.8 _{Vpp} (~ -1 dBFS).					
SFDR	20 MHz 50 MHz 100 MHz 1 MHz 10 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB - 52 dB	Amplitude 1.8 _{Vpp} (~ –1 dBFS). Includes 2nd through the 6th harmonic.					
SFDR	20 MHz 50 MHz 100 MHz 1 MHz 10 MHz 20 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB - 52 dB - 48 dB	Amplitude 1.8 _{VPP} (~ -1 dBFS).					
SFDR	20 MHz 50 MHz 100 MHz 1 MHz 10 MHz 20 MHz 50 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB - 52 dB - 48 dB - 41 dB	Amplitude 1.8 ypp (~ -1 dBFS). Includes 2nd through the 6th harmonic.					
SFDR	20 MHz 50 MHz 100 MHz 1 MHz 20 MHz 50 MHz 100 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB - 52 dB - 48 dB - 41 dB - 36 dB	Amplitude 1.8 _{Vpp} (~ -1 dBFS). Includes 2nd through the 6th harmonic.					
SFDR THD Average Noise	20 MHz 50 MHz 100 MHz 1 MHz 20 MHz 50 MHz 100 MHz 100 MHz	- 49 dBc - 45 dBc - 53 dBc - 56 dB - 52 dB - 48 dB - 41 dB - 36 dB Wrms / √Hz	Amplitudes 1.8 _{Vpp} (~ -1 dBFS). Includes 2nd through the 6th harmonic.					

t, I/O Panel Connector)

	SMB
inge	DC to 105 MHz
solution	1.07 µHz
	0 to 359.978 deg
tion	16384 steps including endpoin
lance	50 Ω ±12%, (DC to 105 MHz)
ction	+8 to -4 V

dpoints

Output	5.0 V	.0 V Level 3.3 V Level 1.8 V Level		Typical			
Current	120	mΑ	72	mA	48 mA		Source or Sink
Amplitude	5.0 V Level		3.3 V Level		1.8 V Level		
(Open Load)	Min	Max	Min	Max	Min	Max	
Vol	-0.10 V	0.40 V	-0.10 V	0.40 V	-0.10 V	0.40 V	
V _{OH}	4.00 V	5.30 V	2.60 V	3.70 V	1.40 V	2.20 V	
Amplitude	5.0 V	Level	3.3 V	Level	1.8 V	Level	If the CHO CLOCK out signal
(50 Load)	Min	Max	Min	Max	Min	Max	is terminated into a 50 Ω load
V _{OL}	-0.10 V	0.20 V	-0.10 V	0.20 V	-0.10 V	0.20 V	the voltage levels will be
V _{OH}	2.00 V	2.65 V	1.30 V	1.85 V	0.70 V	1.10 V	divided by two.

Puty Cycle Bange 25 to 75%
Duty Cycle Accuracy (Typical 1.07 µHz to 60 MHz)
30 to 70% ±2%
25 and 75% ±3%

face, I/O Panel Connector) MB

s an Input	
requency Range	DC to 20 MHz
Direction	Bidirectional
Connector	SMB

..... 1. PXI_Trig <0:7> (Backplane Connector) 2. REF OUT (I/O Panel

	SMB	Connector)	
3.	Start	Trigger	

ut Resistance	1 kΩ ±1%
ut Protection	+8 to -4
	2.0 V
	0.8 V
tput Protection	+8 to -4V

Specifications (continued)

- As an Output		Triggers	
Sources for Output Signal	. 1. PXI_CLK10 (backplane connector)	Туре	Start trigger
	2. Sample timebase clock (60 MHz)	Sources	1. PFI 0 (I/O Panel SMB Connector)
	divided by N ($3 \le N \le 255$)		2. PXI_TRIG<0:7> (backplane connector)
	3. REF IN (I/O panel SMB connector)		3. PXI star trigger (backplane connector)
	PXI_TRIG <0:7> (backplane connector)		4. Software (use function call)
	5. PXI star trigger (backplane connector)		5. Immediate (do not wait for a
	CLOCK output on CH 0		trigger). Default.
	(I/O panel SMB connector)	Mode	Continuous
	7. Software trigger	Trigger Detection	Edge (rising)
	8. Start trigger	Pulse Width (Minimum)	10 ns
Output Impedance	$50 \Omega \pm 5\%$	Trigger to SINE Output Delay	250 μs, typical
Output Protection	. +6 to -1 V	Samula Clock	
V _{OH} (Minimum)		Frequency	200 MS/c
Open load	. 4.0 V	Average Bhase Noise Depaits	300 1013/5
50 Ω load	. 2.0 V	(DLL Reference set to REE IN)	112 dPo/Uz
V _{OL} (Maximum)		(FLL Reference set to REF IN)	10 MHz SINE output
Open load	. 0.4 V		
50 Ω load	. 0.2 V		Oliset to khz ±500 Hz
Rise/Fall Time	. 4 ns	Phase-Lock Loop (PLL)	
REF IN (Reference Innut I/O Panel Conr	nector)	PLL Reference Sources	1. PXI_CLK10 (backplane connector)
Connector	SMB		2. REF IN (I/O panel SMB connector)
Frequency Bange	200 kHz to 30 MHz		3. PXI_TRIG <0:7> (backplane connector)
Destinations	1 PLL reference (refer to		4. None (The PLL is not used. See
	"Phase-Lock Loon (PLL)"		Internal Clock section). Default.
	2 REF OUT (I/O papel SMB connector)	Frequency Accuracy	When using the PLL, the frequency
	3 PELO (I/O panel SMB connector)		accuracy of the NI PXI-5404 is solely
	4 PXL TRIG <0:7> (backplane connector)		dependent on the frequency accuracy
Input Impedance	1 kQ +1%		of the PLL Reference Source.
Input Protection	12 V _m (sine or square wave) +5 VDC	Lock Time	200 ms, typical
Amplitude	300 mVm to 5 Vm	PLL Reference Frequencies	3 to 20 MHz in 1 MHz increments
, an pricedo	Sine or square wave	Frequency Locking Range	±50 ppm
Input Coupling	AC	PLL Reference Duty Cycles	30 to 70%
input oodpiing.		Internal Cleak	
REF OUT (Reference Output, I/O Panel C	connector)		Cleak airquiter cap aither be looked to
Connector	. SMB	CIOCK SOULCE	clock circuity can either be locked to
Frequency Range	DC to 20 MHz		
Sources	. 1. PXI_CLK10 (backplane connector)	Frequency Acouroov	use all onboard frequency reference
	2. Sample timebase (60 MHz)	Frequency Accuracy	±2 ppm, typical for 15 to 35 C
	divided by N ($3 \le N \le 255$).	Frequency Tomporature Coefficient	
	3. REF IN (I/O panel SMB connector)	Frequency remperature coefficient	±0.3 ppm/ C
	4. PXI_TRIG <0:7> (backplane connector)	Multimodule Synchronization	
	5. PXI star trigger (backplane connector)	Output skew of multiple NI 5404s	±1 ns
	6. CH 0 CLOCK output (I/O panel		Note: Two or more PXI-5404s can be
	SMB connector)		programmatically phase-aligned after
	7. PFI 0 (I/O panel SMB connector)		generation has started.
	8. Software trigger	PLL Reference Frequencies for	
	9. Start trigger	Multimodule Synchronization	3, 4, 5, 6, 10, 12, 15, or 20 MHz.
Output Impedance	. 50 Ω ±5 %, DC to 20 MHz	External Calibration (Eastery Calibration	
Output Protection	. +6 to -1 V	Pasammandad Calibratian Interval	1 voor
VOH Open land	4.0.1/	Warm-up time	15 minutes
Open load	. 4.0 V	wann-up une	10 millutes
50 Ω load	. 2.0 V	Power Requirements	
VoL	0.41/	(SINE output, CLOCK output, and REF OU	T generating maximum amplitude
Open load	. U.4 V	waveforms into 50 loads).	
50 Ω load	. U.2 V	+3.3 V	1000 mA
Rise/Fail lime	4 NS	+5 V	550 mA
		+12 V	180 mA
		-12 V	50 mA

Specifications (continued)

Physical	
Dimensions	16.0 by 10.0 cm
(1 3U PXI Slot)	(6.3 by 3.9 in.)
I/O Panel Connectors	
CH0 SINE	SMB male
CH0 CLOCK	SMB male
PFI 0	SMB male
REF IN	SMB male
REF OUT	SMB male
I/O Panel Indicators	
Access LED	Off: Not ready
	Green: Ready to be accessed by software
	Amber: Accessed by computer
	or controller
Active LED	Off: Disabled or in a stopped state
	Red: Error (PLL unlocked or software
	detected an error)
	Green: Generating a waveform
	Amber: Waiting for a trigger

-											
ь	n	v	1	r	n	n	n	n	ρ	n	T
-		٠			U			÷	c		

Operating Temperatu	re	0 to 50 °C
Storage Temperature		-20 to 70 °C

Notes

- 1. Output voltage amplitudes assume a 50 Ω load, unless otherwise noted. 2. SINE output voltage amplitude set to 2 V_{pp} , unless otherwise noted. Load of
- 50 $\boldsymbol{\Omega}$ unless otherwise noted. 3. CLOCK level set to 5 V, unless otherwise noted.
- 4. Typical specifications are determined on a small sampling of PXI-5404 modules.
- 5. Guaranteed by Design specifications are not tested in production.
- 6. 100% tested specifications are measured on every unit.

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