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Requirements and Compatibility | Ordering Information | Detailed Specifications
For user manuals and dimensional drawings, visit the product page resources tab on ni.com.

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NI PXIe-6544, PXIe-6545, PXIe-6547 and NI PXIe-6548

Up to 400 Mbits/s Digital Waveform Generators/Analyzers



- 100/200 MHz maximum clock rate (Up to 200/400 Mbps using double data rate)
- 32 channels with software-selectable per-channel directional control (per cycle direction control on 24 channels on the PXIe-6547/48)
- Voltage levels ranging from 1.2V to 3.3V
- Real-time hardware comparison at up to 200 MHz
- 660 MB/s for acquisition and 400 MB/s for generation - typical data streaming rates
- Onboard direct digital synthesis (DDS)-based high-resolution clock
- NI Synchronization and Memory Core (SMC) device for subnanosecond multidevice synchronization

Overview

The NI PXIe-6544/45/47/48 digital waveform generator/analyzer features 32 bidirectional channels clocked at a maximum of 200 MHz. Voltage levels ranging from 1.2 to 3.3V work with the most common logic levels and are ideal for conducting tests on semiconductor devices, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), ASICs, and microcontrollers. For example, with a 16-bit, parallel interface, 200 MS/s dual-channel DAC, you can use the NI PXIe-6544/45/47/48 to generate data on 32 lines (continuously or in bursts) to test the DAC at its maximum clock rate. You can also pair this device with other NI modular instruments, including digitizers or source measure units (SMUs), to characterize the DAC for various tests at higher rates. Streaming rates of 660 MB/s to host PC memory and 400 MB/s from host PC memory make the NI PXIe-6545/48 ideal for applications requiring high streaming rates. You can use this module to stream high-definition digital video signals for generation or acquisition and to test LCD screens, television components, high-definition signals (up to 1080 p at 60 Hz), RF baseband devices, and HD radio. The NI PXIe-6545/48 also features enhanced timing and synchronization capabilities. The onboard DDS clock provides subhertz resolution up to 200 MHz, helping you clock data (generation or acquisition) with higher precision without using an external clock. In addition, you can now test applications requiring arbitrary clock frequencies and export the onboard clock to other instruments through the backplane of a PXI Express chassis or through an SMB connector on the front panel of the device. Additionally, you can clock your data by importing an external clock through the front panel or backplane. With these features, you can synchronize the NI PXIe-6545/48 with other analog or digital instruments.

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Requirements and Compatibility

OS Information

Windows
Windows 7
Windows 7 64-bit
Windows Vista x64/x86
Windows XP

Driver Information

NI-HSDIO

Software Compatibility

ANSI C/C++
LabVIEW
LabWindows/CVI
Measurement Studio
Measurement Studio .NET Support
Measurement Studio Visual C++ Support
SignalExpress

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Application and Technology

	NI PXI-6544	NI PXIe-6545	NI PXIe-6547	NI PXIe-6548
Max Clock Rate	100 MHz	200 MHz	100 MHz	200 MHz

Max Data Rate	100 Mbits/s	100 Mbits/s	200 Mbits/s (DDR)	400 Mbits/s Generation/ 300 Mbits/s Acquisition (DDR) [1]
Number of Channels	32	32	32	32
Direction Control	Per channel software controlled	Per channel software controlled	Per channel, per cycle, hardware controlled	Per channel, per cycle, hardware controlled
Voltage Levels	1.2, 1.5, 1.8, 2.5, and 3.3 V	1.2, 1.5, 1.8, 2.5, and 3.3 V	1.2 to 3.3 V in 100 mV steps	1.2 to 3.3 V in 100 mV steps
Onboard High-Resolution Clock	Yes	Yes	Yes	Yes
Form Factor	PXI Express	PXI Express	PXI Express	PXI Express
Scripting	Yes	Yes	Yes	Yes
Data Delay	Yes	Yes	Yes, three banks	Yes, three banks
Real-time hardware compare	No	No	Yes on 24 lines	Yes on 24 lines

Table 1. Differences between the different modules

[1]Please refer to the specifications document for more details.

High Signal Quality

NI PXIe-6547/48 modules feature an improved architecture that offers not only higher clock rates up to 200 MHz but also superior signal integrity and impedance matching. You can use them to interface to high-speed digital chips requiring small setup and hold times. At the maximum clock rates of the NI PXIe-6547/48 modules, the signal quality becomes an important feature.

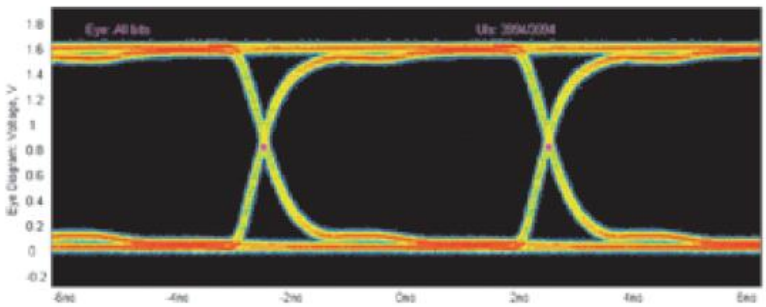


Figure 1. This eye diagram of an NI PXIe-6548 at 200 Mbits/s illustrates a setup including a shielded SHC68-C68-D4 cable with an SMB-2163 terminal block. The oscilloscope being used to acquire the signal is set to 50 Ω input impedance.

High Data-Streaming Rates

With the x4 PXI Express architecture, you can stream at typical rates of 660 MB/s (input) and 400 MB/s (output) to and from a host (PC) or a high-speed storage solution such as the NI HDD-8264 3 TB (RAID) array to onboard memory. You can use these devices to stream high-definition digital video signals for generation or acquisition. You also can test LCD screens, television components, high-definition signals (up to 1080p at 60 Hz), RF baseband devices, and high-definition audio with the NI PXIe-6547/48 modules. With this technology, you can generate terabyte waveforms of unique, high-bandwidth data for several hours. Applications that benefit from this capability include RF and baseband recording and playback for signal intelligence and communications system design, validation, and verification.

Advanced Timing Capabilities

NI PXIe-6547/48 modules also feature enhanced timing and synchronization capabilities. The onboard direct digital synthesis (DDS) clock provides subhertz resolution ranging up to 200 MHz, so you can clock data (generation or acquisition) with higher precision without having to use an external clock. Also, you can now test applications requiring arbitrary clock frequencies with these modules. You can share clocks across the PXI backplane or through an SMA connector on the front panel of the device. You also can clock your data by importing an external clock through the front panel or backplane. With these features, you can synchronize NI PXIe-6547/48 modules with other analog or digital instruments. These modules are built on the Synchronization and Memory Core (SMC), so you can synchronize multiple SMC-based devices (analog or digital) using the NI-TCLK API. You can achieve subnanosecond resolution while synchronizing multiple devices and create highly synchronized high-channel-count systems in a PXI Express chassis.

Advanced Features

Adjust data position (acquisition or generation) to precise locations using the data delay capabilities, which help you adjust your data with respect to the edge of the clock with a resolution of better than 150 ps for all internally generated frequencies.

Link and loop multiple waveforms without any software lag using the scripting features of NI-HSDIO. You can use this feature to write waveforms to the deep onboard memory and then control these waveforms with instructions written in the Script Editor.

Achieve advanced linking, looping, and data streaming with the 64 Mbits per channel (acquisition or generation) and scripting feature of the NI PXIe-6547/48 modules.

Supporting Software

With the NI Digital Waveform Editor, an interactive software tool for creating and editing digital waveforms, you can import test patterns from popular spreadsheet and VHDL simulation packages in ASCII or value change dump (VCD) formats. Once you have imported them, you can view the waveforms graphically and edit them interactively for new devices or new test conditions. You also can build new waveforms with built-in patterns such as pseudorandom bit sequences (PRBS) and count up/down patterns. When you are ready to test your device, you can seamlessly import the waveforms into LabVIEW, LabVIEW SignalExpress, and ANSI C. The Digital Waveform Editor is included with the 8 and 64 Mbits per channel memory models and is a separate add-on for use with the 1 Mbit per channel model.

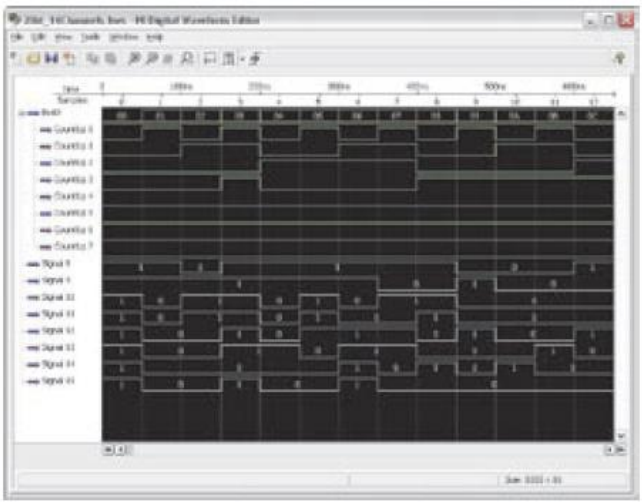


Figure 2. Create and edit digital waveforms using the NI Digital Waveform Editor.

With the NI-HSDIO driver, you can use NI PXIe-6547/48 modules with graphical programming languages such as NI LabVIEW or text-based languages such as NI LabWindows™/CVI or ANSI C.

You can even use these modules in a nonprogramming environment such as LabVIEW SignalExpress. With the intuitive LabVIEW SignalExpress environment, you can generate, acquire, and perform advanced capabilities such as hardware comparisons. You also can use LabVIEW SignalExpress for digital processing functions.

Connectivity

To meet connectivity requirements for high-speed digital applications, you can use NI PXIe-6547/48 modules with a variety of accessories such as the following:

NI CB-2162 connector block
Shielded 50 Ω flying-lead cable
VHDCI high-density connector

Tight Synchronization Capabilities

The PXI Express backplane offers a built-in common reference clock for the synchronization of multiple digital instruments in a system. You can synchronize multiple analog and digital modules on a picosecond level using the PXI platform. Figure 3 shows how you can synchronize multiple analog and digital instruments using the trigger and clock routes on the PXI backplane.

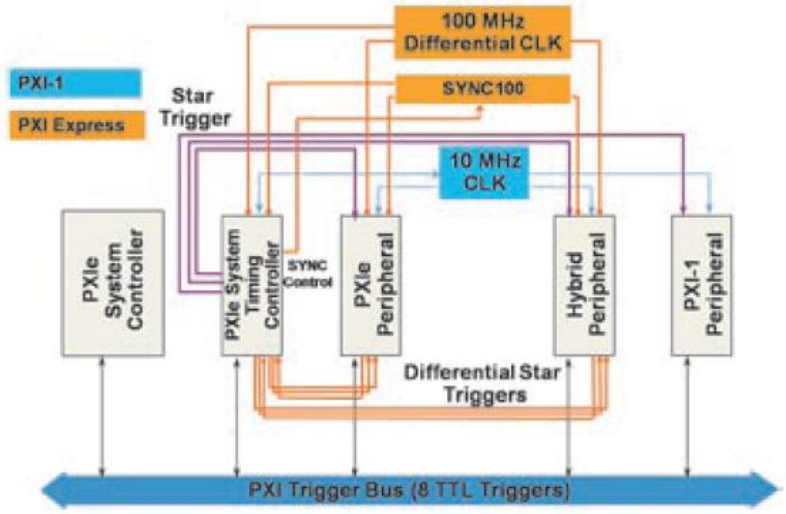


Figure 3. You can use the backplane of a PXI chassis to route triggers and clocks for channel expansion or mixed-signal synchronization.

Applications

With these features, you can perform tests on semiconductor devices such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), ASICs, and microcontrollers. For example, with a 16-bit, parallel interface, 200 MS/s dual-channel DAC, you can use the NI PXIe-6548 to generate data on 32 lines (continuously or in bursts) to test the DAC at its maximum clock rate. With the selectable voltages, you can test digital devices, which need logic levels that traditional instruments cannot provide. You can also pair the NI PXIe-6548 with other NI modular instruments such as digitizers or source measure units (SMUs) to characterize the DAC for various tests including spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), intermodulation distortion (IMD), integral nonlinearity (INL), and differential nonlinearity (DNL) tests at higher rates. Figure 4 shows the front panel of a dynamic characteristics test implemented in LabVIEW.

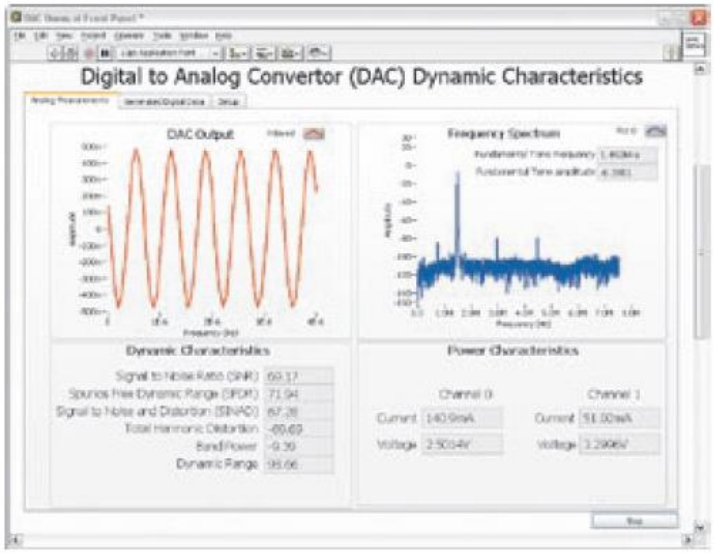


Figure 4. SFDR of a 200 MS/s DAC Using the NI PXIe-6548

Easy Integration with Other PXI-Based Instruments

Test systems typically contain many instrument types, including signal sources, measurement devices, and switches. The PXI platform has unparalleled breadth, with modules for analog and digital I/O, high-speed instrumentation, vision, motion, and numerous bus interfaces. More than 1,500 PXI modules are available from the more than 70 members of the PXI Systems Alliance (PXISA). This means you can build a comprehensive test system in a single chassis as well as synchronize modules in that chassis to picosecond-level accuracy when using NI modular instrumentation. In addition, you can use an NI PXIe-6547/48 module with other instruments such as digitizers, power supplies, and switches to create a flexible and powerful mixed-signal test system.

Advanced Features on the PXIe-6547 and PXIe-6548

Hardware Compare: These boards feature onboard, real-time hardware compare. This feature is ideal for a stimulus/response type application. You can send a stimulus waveform to a device under test (DUT) and compare response data, either on the same channel or on other input channels. This feature combined with per cycle direction control allows for bit error rate testing, custom protocol communication such as SPI, I2C and JTAG or stimulus response tests.

Multiple Banks of Data Delay: The PXIe-6547 and PXIe-6548 feature three banks of data delay. You can phase shift data lines with a resolution of 150 ps (worst case), to account for load board trace lengths, rise/fall/setup and hold times or ringing on digital signals. You can also use the synchronization capabilities of the digital devices coupled with data delay features to get even more data delay banks across multiple boards. You can also select the synchronization offset between multiple boards using the NI-TCLK API.

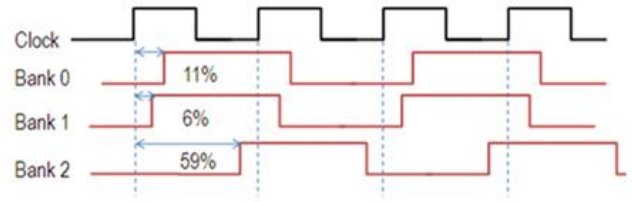


Figure 5: Multiple banks of data delay on the PXIe-6547/48 allow for phase shifting of data channels with respect to the clock.

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Ordering Information

For a complete list of accessories, visit the product page on ni.com.

Products	Part Number	Recommended Accessories	Part Number
NI PXIe-6548			
NI PXIe-6548- 1 Mb/ch Each NI PXIe-6548- 1 Mb/ch requires: 1 Cable, 1 Connector Block	781012-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6548- 8 Mb/ch Each NI PXIe-6548- 8 Mb/ch requires: 1 Cable, 1 Connector Block	781012-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6548- 64 Mb/ch Each NI PXIe-6548- 64 Mb/ch requires: 1 Cable, 1 Connector Block	781012-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162	778592-01

		***Also available: PCB Mountable Connectors*	
NI PXIe-6547			
NI PXIe-6547- 1 Mb/ch Each NI PXIe-6547- 1 Mb/ch requires: 1 Cable, 1 Connector Block	781011-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6547- 8 Mb/ch Each NI PXIe-6547- 8 Mb/ch requires: 1 Cable, 1 Connector Block	781011-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6547- 64 Mb/ch Each NI PXIe-6547- 64 Mb/ch requires: 1 Cable, 1 Connector Block	781011-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6545			
NI PXIe-6545-8 Mb/ch Each NI PXIe-6545-8 Mb/ch requires: 1 Cable, 1 Connector Block	780993-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6545-64 Mb/ch Each NI PXIe-6545-64 Mb/ch requires: 1 Cable, 1 Connector Block	780993-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6545-1 Mb/ch Each NI PXIe-6545-1 Mb/ch requires: 1 Cable	780993-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
NI PXIe-6544			
NI PXIe-6544- 1 Mb/ch Each NI PXIe-6544- 1 Mb/ch requires: 1 Cable, 1 Connector Block	780992-01	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6544- 8 Mb/ch Each NI PXIe-6544- 8 Mb/ch requires: 1 Cable, 1 Connector Block	780992-02	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01
NI PXIe-6544-64 Mb/ch Each NI PXIe-6544-64 Mb/ch requires: 1 Cable, 1 Connector Block	780992-03	**Cable:** Single-Ended - SHC68-C68-D4 Cable (1m) ***Also available: Shielded*	196275-01
		Connector Block: Single Ended High-Speed Digital Connector Blocks - CB-2162 ***Also available: PCB Mountable Connectors*	778592-01

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

Support - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
Discussion Forums - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
Online Community - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

Classroom training in cities worldwide - the most comprehensive hands-on training taught by engineers.
On-site training at your facility - an excellent option to train multiple employees at the same time.
Online instructor-led training - lower-cost, remote training if classroom or on-site courses are not possible.
Course kits - lowest-cost, self-paced training that you can use as reference guides.
Training memberships and training credits - to buy now and schedule training later.
Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

100/200 MHz Digital Waveform Generator/Analyzer

This document provides the specifications for the NI PXIe-6544 (NI 6544), NI PXIe-6545 (NI 6545), NI PXIe-6547 (NI 6547), and NI PXIe-6548 (NI 6548).

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Typical specifications are unwarranted values that are representative of a majority (3σ) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Nominal specifications are unwarranted values that are relevant to the use of the product and convey the expected performance of the product.

These specifications are valid within the operating temperature range. Specifications are subject to change without notice. For the most recent NI 6544/6545/6547/6548 specifications, visit ni.com/manuals.

To access the NI 6544/6545/6547/6548 documentation, including the *NI Digital Waveform Generator/Analyzer Getting Started Guide*, which contains functional descriptions of the NI 6544/6545/6547/6548 signals and the connector pinouts, navigate to **Start » Programs » National Instruments » NI-HSDIO » Documentation**.

Hot Surface If the NI 6544/6545/6547/6548 has been in use, it may exceed safe handling temperatures and cause burns. Allow time to cool before removing the NI 6544/6545/6547/6548 from the chassis.

Channel Specifications

Specification	Value		Comments
Number of data channels	**NI 6544/6545**	**NI 6547/6548**	Data rate multiplier is software selectable to be SDR or DDR. Using SDR, data is clocked using the rising or falling edge of the Sample clock. Using DDR, data is clocked using both edges of the Sample clock.
	32 single data rate (SDR) channels	32 single data rate (SDR) channels *or* 16 double data rate (DDR) channels per direction **Note** Generation and acquisition sessions may be independently configured for DDR operation on either the lower data channels (<0:15>) or the upper data channels (<16:31>).	
Direction control of data channels	Per channel, per operation	Per channel, per cycle	—
Number of programmable function interface (PFI) channels	4		Refer to the *Waveform Specifications* section for more details.
Direction control of PFI channels	Per channel		—
Number of clock terminals	2 input, 2 output		Refer to the *Timing Specifications* section for more details.

Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)

Specification	Value					Comments
Generation signal type	Single-ended					—
Number of programmable generation voltage levels	1 Voltage high level (V_{OH}) Generation Voltage Low Level (V_{OL}) is always set to 0 V. **Note** Generation and acquisition sessions share a common programmable voltage resource. For simultaneous operations, acquisition thresholds must be set to half of the Generation Voltage High Level setting.					NI 6547/ 6548 only; for all data, PFI, and clock channels.
Generation voltage range	1.2 V to 3.3 V					
Generation voltage resolution	100 mV					
DC generation voltage accuracy	**Typical**		**Maximum**			Into 1 MΩ; does not include system crosstalk.
	±35 mV		±200 mV			
Generation logic families	1.2V, 1.5V, 1.8V, 2.5V, 3.3V Logic Families Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.					All devices; for all data, PFI, and clock channels. Nominal values have ±35 mV typical accuracy with a 100 µA load. Does not include system crosstalk.
Generation voltage levels	**Logic Family**	**Voltage Low Levels**		**Voltage High Levels**		
		Nominal	**Max**	**Min**	**Nominal**	
	1.2V (V_{OH} = 1.2 V)	0.0 V	0.2 V	1 V	1.2 V	
	1.5V (V_{OH} = 1.5 V)	0.0 V	0.2 V	1.3 V	1.5 V	
	1.8V (V_{OH} = 1.8 V)	0.0 V	0.2 V	1.6 V	1.8 V	
	2.5V (V_{OH} = 2.5 V)	0.0 V	0.2 V	2.3 V	2.5 V	
	3.3V (V_{OH} = 3.3 V)	0.0 V	0.2 V	3.1 V	3.3 V	
Output impedance	50 Ω					Nominal.
Maximum allowed DC drive strength	**Logic Family**		**Maximum Allowed DC Drive Strength**			Nominal.
	1.2V		±12 mA			
	1.5V		±15 mA			
	1.8V		±18 mA			
	2.5V		±25 mA			
	3.3V		±33 mA			
Data channel driver enable/ disable control	Per channel					Software-selectable.
Channel power-on state	Drivers disabled, 50 kΩ nominal input impedance					—
Output protection	The device can indefinitely sustain a short to any voltage between 0 V and 5 V.					—

Acquisition Channels (Data, STROBE, and PFI <0..3>)

Specification	Value			Comments
Acquisition signal type	Single-ended			—
Number of programmable acquisition thresholds	1 voltage threshold (V_{IH} = V_{IL}) **Note** Generation and acquisition sessions share a common programmable voltage resource. For simultaneous operations, Generation Voltage High Level must be set to twice the Acquisition Threshold.			NI 6547/6548 only; for all data, PFI, and clock channels.
Acquisition Voltage Threshold Range	0.6 V to 1.65 V			
Acquisition voltage threshold resolution	50 mV			
DC acquisition voltage threshold accuracy	**Typical**	**Maximum**		Does not include system crosstalk.
	±150 mV	±30%		
Acquisition logic families	1.2V, 1.5V, 1.8V, 2.5V, 3.3V, Logic Families **Note** Generation and acquisition sessions share a common voltage resource. Simultaneous operations must be set to the same logic family.			All devices; for all data, PFI, and clock channels. Does not include system crosstalk.
~~Acquisition voltage~~	~~**Logic Family**~~	~~**Voltage Thresholds Low**~~	~~**Voltage Thresholds High**~~	

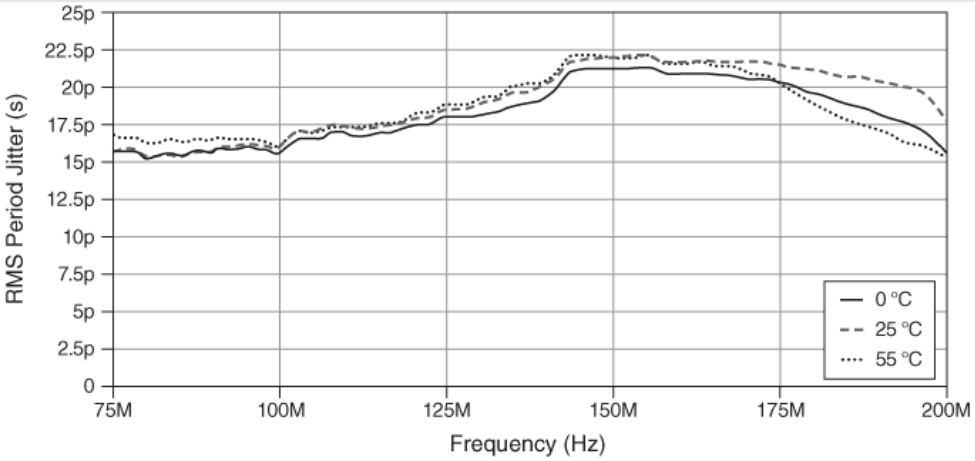
Specification	Value					Comments
thresholds		**Min**	**Typical**	**Typical**	**Max**	
	1.2V (V_{IH}, V_{IL} = 0.60 V)	420 mV	450 mV	750 mV	780 mV	
	1.5V (V_{IH}, V_{IL} = 0.75 V)	525 mV	600 mV	900 mV	975 mV	
	1.8V (V_{IH}, V_{IL} = 0.90 V)	630 mV	750 mV	1.05 V	1.17 V	
	2.5V (V_{IH}, V_{IL} = 1.25 V)	875 mV	1.10 V	1.40 V	1.625 V	
	3.3V (V_{IH}, V_{IL} = 1.65 V)	1.155 V	1.50 V	1.80 V	2.145 V	
Input impedance	High-impedance (50 kΩ)					Nominal.
Input protection	–1 V to 5 V					Internal diode clamps may begin conduction outside the –0.5 V to 3.5 V range.

Timing Specifications

Sample Clock

Specification	Value		Comments
Sample clock sources	1. On Board Clock (internal 800 MHz VCO with 16-bit DDS) 2. CLK IN (SMA jack connector) 3. STROBE (Digital Data & Control (DDC) connector; acquisition only)		—
On Board Clock frequency range	**NI 6544**, **NI 6547**: 100 Hz to 100 MHz **NI 6545**, **NI 6548**: 100 Hz to 200 MHz		—
On Board Clock frequency resolution	0.2 Hz maximum **Note** Varies with Sample clock frequency.		NI-HSDIO may be queried for the programmed frequency value.
On Board Clock frequency accuracy	±150 ppm + 5 ppm per year		Accuracy may be increased by using a higher performance external Reference clock.
CLK IN frequency range	**NI 6544**, **NI 6547**: 20 kHz to 100 MHz **NI 6545**, **NI 6548**: 20 kHz to 200 MHz		Refer to the *CLK IN (SMA Jack Connector)* section for restrictions based on waveform type.
STROBE frequency range	**NI 6544**, **NI 6547**: 100 Hz to 100 MHz **NI 6545**, **NI 6548**: 100 Hz to 200 MHz		Refer to the *STROBE (DDC Connector)* section.
Sample clock relative delay adjustment range	0.0 to 1.0 Sample clock period (acquisition sessions) 0.0 ns to 5.0 ns (generation sessions)		You can apply a delay or phase adjustment to the On Board Clock to align multiple devices.
Sample clock relative delay adjustment resolution	0.5 ps		
Exported Sample clock destinations	1. DDC CLK OUT (DDC connector) 2. CLK OUT (SMA jack connector)		Internal Sample clocks with sources other than STROBE can be exported.
Exported Sample clock delay range	0.0 to 1.0 Sample clock periods		Resolution is nonlinearly dependent on clock frequency and may be queried for by using NI-HSDIO.
Exported Sample clock delay resolution (δ_C)	117 ps to 143 ps Nominal		
Exported Sample Clock delay frequency	**On Board Clock**	**External Clock**	
	All supported frequencies	Frequencies ≥ 20 MHz	
Exported Sample clock jitter	**Period Jitter**	**Cycle-to-Cycle Jitter**	Characteristic; using On Board Clock.
	24 ps_{rms}	43 ps_{rms}	

Characteristic Period Jitter (RMS) vs. Frequency

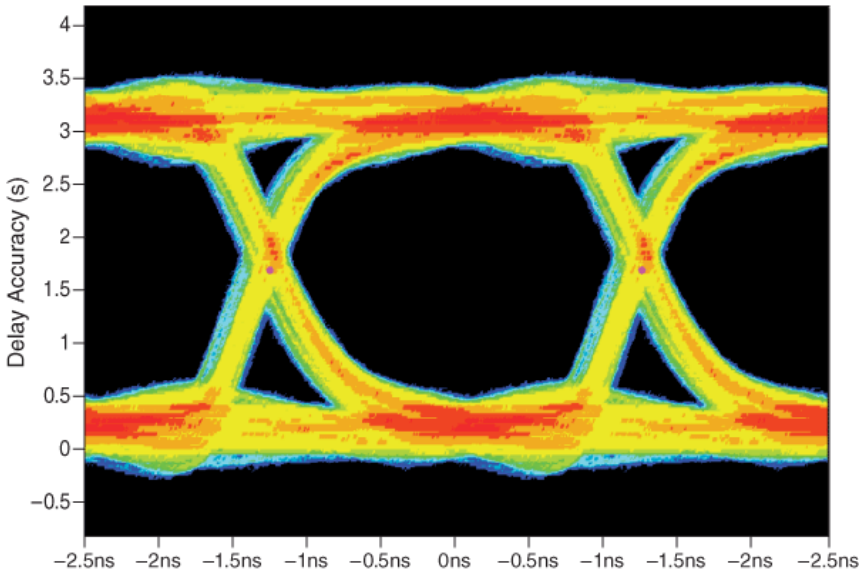


Specification	Value					Comments
Exported Sample Clock Duty Cycle	**Logic Family**	**DDC Clock Out**		**SMA Clock Out**		NI 6545/6548 at maximum clock rate (200 MHz) Not including the effects of system crosstalk.
		Min	**Max**	**Min**	**Max**	
	1.2V	37%	50%	35%	47%	
	1.5V	41%	53%	36%	48%	
	1.8V	42%	55%	39%	51%	
	2.5V	45%	57%	41%	54%	
	3.3V	48%	58%	43%	55%	

Generation Timing (Data, DDC CLK OUT, and PFI <0..3> Channels)

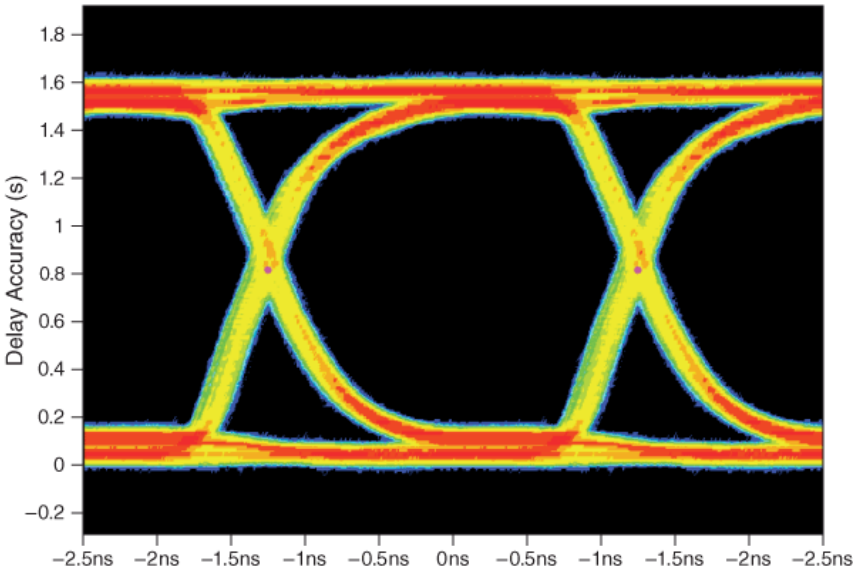
Specification	Value				Comments
Data channel-to-channel skew	±300 ps				Maximum skew across all data channels, PFI channels, and voltage levels.
Maximum Data Rate per Channel	**NI 6544**	SDR: 100 Mbps Supported for all logic families.			Includes maximum data channel-to-channel skew and typical crosstalk. NI 6547/6548 devices generate two samples per clock cycle in DDR mode.
	NI 6545	SDR: 200 Mbps Supported for all logic families.			
	NI 6547	SDR: 100 Mbps DDR: 200 Mbps Supported for all logic families and selectable voltage levels.			
	NI 6548	**Logic Family**	**SDR**	**DDR**	
		3.3V	200 Mbps	400 Mbps	
		2.5V		400 Mbps	
		1.8V		375 Mbps	
		1.5V		350 Mbps	
		1.2V		300 Mbps	
		Voltage Levels	**SDR**	**DDR**	
		2.5 V to 3.3 V	200 Mbps	400 Mbps	
		1.8 V to 2.4 V		375 Mbps	
		1.5 V to 1.7 V		350 Mbps	
		1.2 V to 1.4 V		300 Mbps	

Characteristic Eye Diagram (high impedance)



The preceding figure, *Characteristic Eye Diagram (high impedance)*, shows an eye diagram of a 400 Mbps pseudorandom bit sequence (PRBS) waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into high impedance.

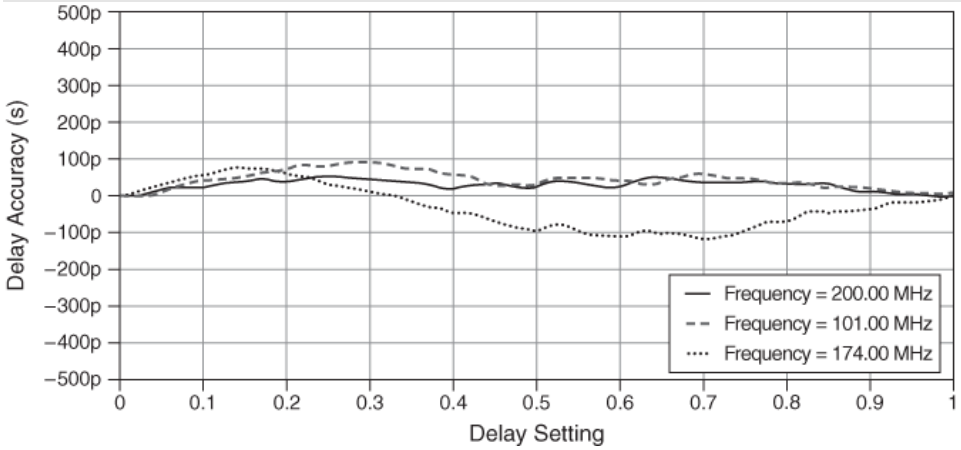
Characteristic Eye Diagram (50 Ω Termination)



The preceding figure, *Characteristic Eye Diagram (50 Ω Termination)*, shows an eye diagram of a 400 Mbps PRBS waveform in DDR mode at 3.3 V. This waveform was captured on DIO 0 at room temperature into 50 Ω termination.

Specification	Value		Comments
Data position modes	Sample clock rising edge, Sample clock falling edge, or Delay from Sample clock rising edge		—
Generation data delay range (δ_G)	0.0 to 1.0 Sample clock periods		Resolution is nonlinearly dependent on clock frequency and may be queried for using NI-HSDIO.
Generation data delay resolution (δ_G)	117 ps to 143 ps nominal		
Generation data delay frequency	**On Board Clock**	**External Clock**	
	All supported frequencies	Frequencies ≥ 20 MHz	

Characteristic Data Delay Accuracy



Specification	Value	Comments
Exported Sample clock offset (t_{CO})	0.0 ns or 1.65 ns (default)	Nominal; Software selectable for DDC_CLK_ OUT.
Time delay from Sample clock (internal) to DDC connector (t_{SCDDC})	8.1 ns	Characteristic; Exported Sample clock offset = 0 ns

Generation Provided Setup and Hold Times

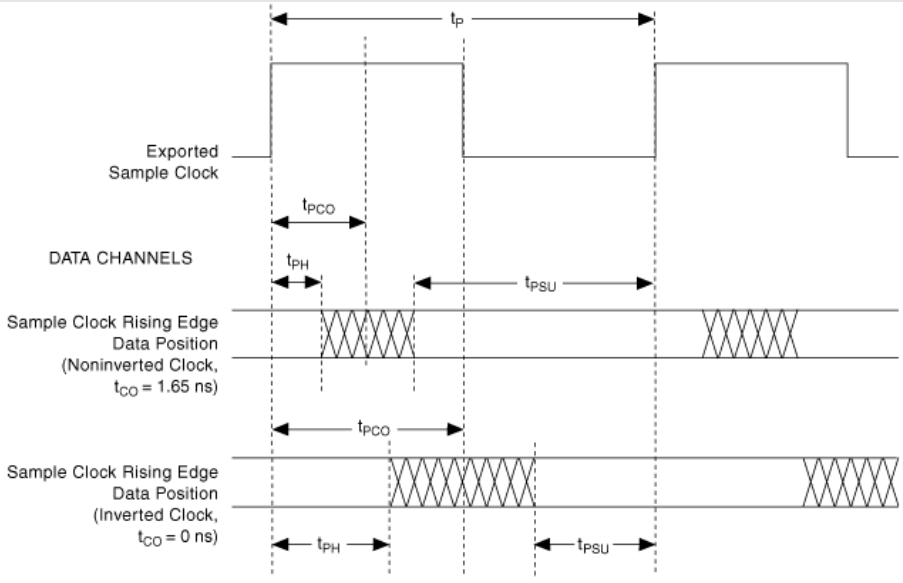
Exported Sample Clock Offset (t_{PCO})	Minimum Provided Setup Time (t_{PSU})	Minimum Provided Hold Time (t_{PH})
1.65 ns	tp – 2.15 ns	1.15 ns
0.0 ns	tp – 500 ps	–500 ps

Compare the setup and hold times from the datasheet of your device under test (DUT) to the values in the table above. The provided setup and hold times must be greater than the setup and hold times required for the DUT. If you require more setup time, configure your exported Sample clock mode to Inverted and/or delay your clock or data relative to the Sample clock.

Refer to the *Generation Provided Setup and Hold Times Timing Diagram* for an illustration of the relationship between the exported Sample clock mode and the provided setup and hold times.

Note This table assumes the data position is set to Sample clock rising edge and the noninverted Sample clock is exported to the DDC connector. This table includes worst-case effects of channel-to-channel skew and intersymbol interference.

Generation Provided Setup and Hold Times Timing Diagram



$t_P = \frac{1}{f}$ = Sample Clock Period

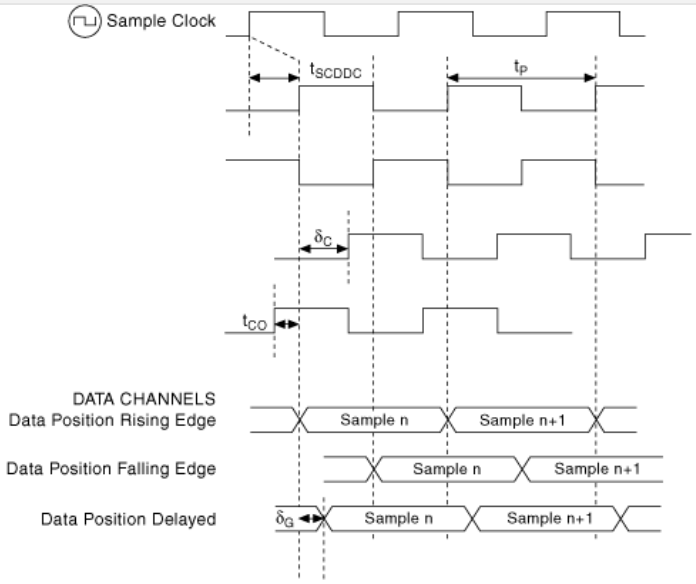
t_{PH} = Minimum Provided Hold Time

t_{PSU} = Minimum Provided Set-Up Time

t_{PCO} = Time from Rising Clock Edge to Data Transition (Provided Clock to Out Time)

t_{CO} = Exported Sample Clock Offset

Generation Timing Diagram



t_{SCDDC} : Time Delay from Sample Clock (Internal) to DDC Connector

$0 \le \delta_C \le 1$: Exported Sample Clock Delay (Fraction of t_P)

$0 \le \delta_G \le 1$: Pattern Generation Data Delay (Fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

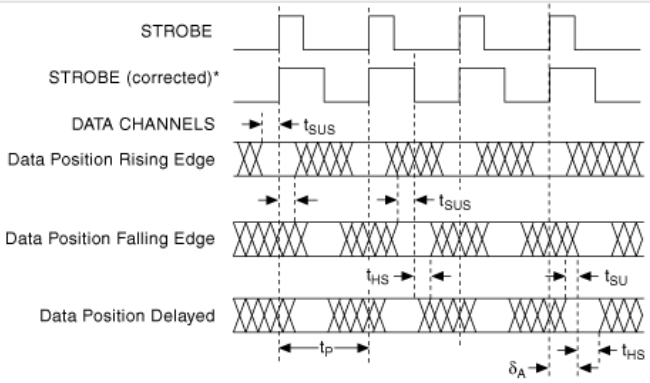
t_{CO} = Exported Sample Clock Offset; 1.65 ns, Software-Selectable

Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)

Specification	Value				Comments
Channel-to-channel skew	±350 ps				Maximum skew across all data channels, PFI channels, and voltage levels.
Maximum Data Rate per Channel	**NI 6544**	SDR: 100 Mbps Supported for all logic families.			Includes maximum data channel-to-channel skew and typical crosstalk. NI 6547/6548 devices acquires two samples per clock cycle in DDR mode.
	NI 6545	SDR: 200 Mbps Supported for all logic families.			
	NI 6547	SDR: 100 Mbps DDR: 200 Mbps Supported for all logic families and selectable voltage levels.			
	NI 6548	**Logic Family**	**SDR**	**DDR**	
		3.3V	200 Mbps	300 Mbps	
		2.5V		300 Mbps	
		1.8V		250 Mbps	
		1.5V		225 Mbps	
		1.2V		200 Mbps	
		Voltage Threshold	**SDR**	**DDR**	
		1.25 V to 1.65 V	200 Mbps	300 Mbps	
		0.90 V to 1.20 V		250 Mbps	
		0.75 V to 0.85 V		225 Mbps	
		0.60 V to 0.70 V		200 Mbps	

<table>
<tr><th>Specification</th><th colspan="5">Value</th><th>Comments</th></tr>
<tr><td rowspan="6">Setup and Hold Times to STROBE</td><td rowspan="2">Voltage Threshold</td><td colspan="2">Hold Time (t_{hs})</td><td colspan="2">Setup Times (t_{sus})</td><td rowspan="6">Characteristic includes maximum data channel-to-channel skew and uncertainty, but does not include system crosstalk. Performance may vary with system crosstalk performance.</td></tr>
<tr><td>< 20 MHz</td><td>≥ 20 MHz</td><td>< 20 MHz</td><td>≥ 20 MHz</td></tr>
<tr><td>1.25 V to 1.65 V</td><td rowspan="4">2.4 ns</td><td>900 ps</td><td rowspan="4">2.8 ns</td><td>1.15 ns</td></tr>
<tr><td>0.90 V to 1.20 V</td><td>1.00 ns</td><td>1.20 ns</td></tr>
<tr><td>0.75 V to 0.85 V</td><td>1.10 ns</td><td>1.40 ns</td></tr>
<tr><td>0.60 V to 0.70 V</td><td>1.25 ns</td><td>1.75 ns</td></tr>
<tr><td>Data position modes</td><td colspan="5">Sample clock rising edge, Sample clock falling edge, or Delay from Sample clock rising edge.</td><td>—</td></tr>
<tr><td>Acquisition data delay range</td><td colspan="5">0.0 to 1.0 Sample clock periods</td><td rowspan="3">Resolution is nonlinearly dependent on clock frequency and may be queried for by using NI-HSDIO.</td></tr>
<tr><td>Acquisition data delay resolution</td><td colspan="5">117 ps to 143 ps nominal</td></tr>
<tr><td rowspan="2">Acquisition data delay frequency</td><td colspan="2">On Board Clock</td><td colspan="3">External Clock and STROBE</td></tr>
<tr><td colspan="2">All supported frequencies</td><td colspan="3">Frequencies ≥ 20 MHz</td></tr>
<tr><td>Setup time to sample clock (t_{susc})</td><td colspan="5">900 ps</td><td rowspan="2">Nominal; does not include channel-to-channel skew, t_{DDCSC}, or t_{SCDDC}.</td></tr>
<tr><td>Hold time to sample clock (t_{HSC})</td><td colspan="5">425 ps</td></tr>
<tr><td>Time delay from DDC connector to internal sample clock</td><td colspan="5">6.8 ns</td><td>Nominal.</td></tr>
</table>

Acquisition Timing Diagram Using STROBE as the Sample Clock



t_{SUS} = Set-Up Time to STROBE

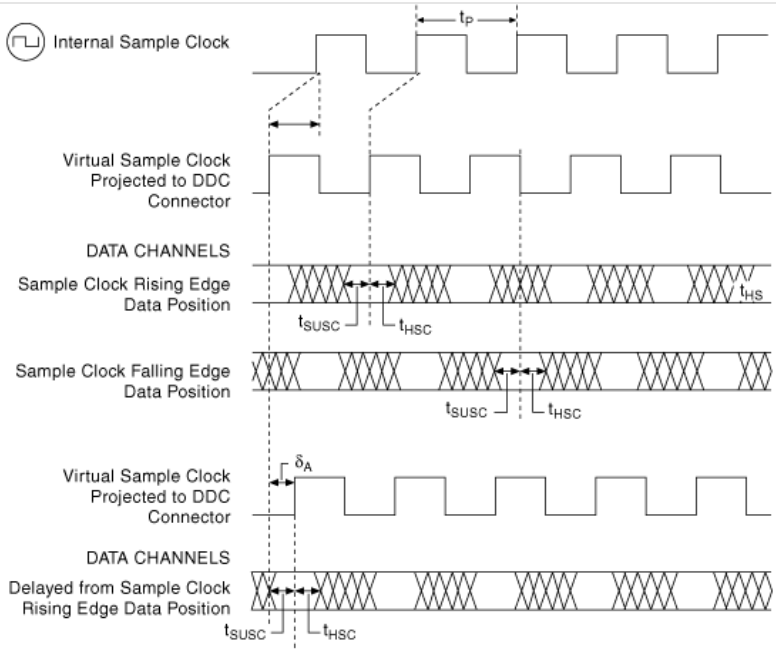
t_{HS} = Hold Time from STROBE

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Sample Clock Period

*Note: When using an external sample clock greater than 20 MHz, the duty cycle is corrected to 50%.

Acquisition Timing Diagram with Sample Clock Sources Other than STROBE



t_{DDCSC} : Time Delay from DDC Connector to Internal Sample Clock

$0 \le \delta_A \le 1$: Acquisition Data Delay (fraction of t_P)

$t_P = \frac{1}{f}$ = Period of Sample Clock

t_{SUSC} = Set-Up Time to Sample Clock

t_{HSC} = Hold Time to Sample Clock

CLK IN (SMA Jack Connector)

Specification	Value					Comments
Direction	Input to device					—
Destinations	1. Reference clock - for the phase lock loop (PLL) 2. Sample clock					—
Input coupling	AC					—
Input protection	±10 VDC					Nominal.
Input impedance	50 Ω (default) or 1 kΩ					Software-selectable; Nominal.
Minimum detectable pulse width	2 ns					Nominal.
Clock requirements	Clock must be continuous and free-running.					—
Voltage Ranges	**Square Waves**					—
	0.65 V_{pp} to 5.0 V_{pp}					
	Sine Waves					—
	Voltage range	0.65 V_{pp} to 5.0 V_{pp}	1.0 V_{pp} to 5.0 V_{pp}	1.3 V_{pp} to 5.0 V_{pp}	2.6 V_{pp} to 5.0 V_{pp}	
	Frequency range	20 MHz to 100 MHz	13 MHz to 100 MHz	10 MHz to 100 MHz	5 MHz to 100 MHz	Supported by NI 6544 and 6547 only.
		20 MHz to 200 MHz	13 MHz to 200 MHz	10 MHz to 200 MHz	5 MHz to 200 MHz	Supported by NI 6545 and 6548 only.
As Sample Clock						
Frequency range	NI 6544 and NI 6547: 20 kHz to 100 MHz NI 6545 and NI 6548: 20 kHz to 200 MHz					Nominal 3 dB cutoff point at 100 MHz when using 1 kΩ input impedance.
Duty cycle range	f < 20 MHz: 25% to 75% f ≥ 20 MHz: 40% to 60%					—
As Reference Clock						
Reference clock frequency range	5 MHz to 100 MHz (Integer multiples of 1 MHz)					—

Specification	Value	Comments
Reference clock frequency accuracy	± 0.1%	Required accuracy of the external Reference clock source.
Reference clock duty cycle	25% to 75%	—

STROBE (DDC Connector)

Specification	Value	Comments
Direction	Input to device	—
Destinations	Sample clock (acquisition only)	—
STROBE frequency range	**NI 6544, NI 6547:** 100 Hz to 100 MHz **NI 6545, NI 6548:** 100 Hz to 200 MHz	—
STROBE duty cycle range	35% to 65% for clock frequencies ≥ 20 MHz 25% to 75% for clock frequencies < 20 MHz **Note** STROBE duty cycle is corrected to 50% at frequencies ≥ 20 MHz.	Duty cycle at the programmed threshold.
Minimum detectable pulse width	1.75 ns	Nominal; required at acquisition voltage thresholds.
Voltage thresholds	Refer to the *Acquisition Timing (Data, STROBE, and PFI <0..3> Channels)* specifications in the *Channel Specifications* section.	—
Clock requirements	Clock must be continuous and free-running.	—
Input impedance	50 kΩ	Nominal.

CLK OUT (SMA Jack Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	1. Sample clock (excluding STROBE) 2. Reference clock (PLL)	—
Output impedance	50 Ω	Nominal.
Electrical characteristics	Refer to the *Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)* specifications in the *Channel Specifications* section.	—
Logic type	Matched with generation and acquisition sessions.	—

DDC CLK OUT (DDC Connector)

Specification	Value	Comments
Direction	Output from device	—
Sources	Sample clock (generation only)	STROBE and acquisition Sample clock cannot be routed to DDC CLK OUT.
Electrical characteristics	Refer to the *Generation Channels (Data, DDC CLK OUT, and PFI <0..3>)* specifications in the *Channel Specifications* section.	—

Reference Clock (PLL)

Specification	Value	Comments
Reference clock sources	1. PXI_CLK100 (PXI Express backplane) 2. CLK IN (SMA jack connector) 3. None (internal oscillator locked to an internal reference)	Provides the reference frequency for the PLL.
Lock time	150 ms	Maximum, not including software latency.
Reference clock frequencies	5 MHz to 100 MHz (integer multiple of 1 MHz)	0.1% required accuracy.
Reference clock duty cycle range	25% to 75%	—

Specification	Value	Comments
Reference clock destinations	CLK OUT (SMA jack connector)	—

Waveform Specifications

Memory and Scripting

Specification	Value			Comments
Memory architecture	The NI 6544/6545/6547/6548 uses the Synchronization and Memory Core (SMC) technology in which waveforms and instructions share onboard memory. Parameters such as number of script instructions, maximum number of waveforms in memory, and number of samples (S) available for waveform storage are flexible and user-defined.			Refer to the *Onboard Memory* section in the *NI Digital Waveform Generator/Analyzer Help* for more information.
Onboard memory size (generation and acquisition)	1 Mbit/channel	8 Mbit/channel	64 Mbit/channel	Maximum limit for generation sessions assumes no scripting instructions.
Generation modes	**Single-waveform mode:** Generate a single waveform once, *n* times, or continuously.			—
	Scripted mode: Generate a simple or complex sequence of waveforms. Use scripts to describe the waveforms to be generated, the order in which the waveforms are generated, how many times the waveforms are generated, and how the device responds to Script triggers.			
Generation minimum waveform size in samples (S)	**Configuration**	**Sample Rate**		Sample rate dependent. Increasing sample rate increases minimum waveform size requirement. For information on these configurations, refer to *Common Scripting Use Cases* in the *NI Digital Waveform Generator/ Analyzer Help*.
		200 MHz (NI 6545/6548 Only)	**100 MHz**	
	Single waveform	1 S	1 S	
	Continuous waveform	128 S	64 S	
	Stepped sequence	128 S	64 S	
	Burst sequence	1056 S	512 S	
Generation finite repeat count	1 to 16,777, 216			—
Generation waveform quantum	**Data Width = 4**	**Data Width = 2**		DDR mode sets data width to 2.
	1 sample	2 samples		
Generation waveform block size (in physical memory)	**Data width = 4**	**Data width = 2**		—
	32 samples	64 samples		
Acquisition minimum record size	1 S			Regardless of waveform size, NI-HSDIO allocates at least 640 bytes for a record.
Acquisition record quantum	1 S			—
Acquisition maximum number of records	2,147,483,647			Session should fetch fast enough so that unfetched data is not overwritten.
Acquisition number of pre-Reference trigger samples	0 up to full record			—
Acquisition number of post-Reference trigger samples	0 up to full record			—

Triggers (Inputs to the NI 6544/6545/6547/6548)

Specification	Value	Comments
Trigger types	1. Start trigger 2. Pause trigger	—

Specification	Value	Comments
	3. Script trigger <0..3> (generation sessions only) 4. Reference trigger (acquisition sessions only) 5. Advance trigger (acquisition sessions only) 6. Stop Trigger (generation sessions only)	
Sources	1. PFI 0 (SMA jack connector) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..7> (PXI Express backplane) 4. Pattern match (acquisition sessions only) 5. Software (user function call) 6. Disabled (do not wait for a trigger)	—
Trigger detection	1. Start trigger (edge detection: rising or falling) 2. Pause trigger (level detection: high or low) 3. Script trigger <0..3> (edge detection: rising or falling; level detection: high or low) 4. Reference trigger (edge detection: rising or falling) 5. Advance trigger (edge detection: rising or falling) 6. Stop Trigger (edge detection: rising or falling)	—
Minimum required trigger pulse width	15 ns	—
Destinations	1. PFI 0 (SMA jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI Express backplane)	Each trigger can be routed to any destination except the Pause trigger. The Pause trigger cannot be exported.
Trigger rearm time	**Start to Reference Trigger**: 150 s **Start to Advance Trigger**: 220 s **Advance to Advance Trigger**: 220 s **Reference to Reference Trigger**: 220 s	Maximum number of samples.
Delay from Pause trigger to Pause state and Stop trigger to Done state.	**Generation Sessions**: 50 Sample clock periods + 300 ns **Acquisition Sessions**: Synchronous with the data	Maximum; Use the Data Active event during generation to determine on a sample by sample basis when the device enters the Pause or Done states.
Delay from trigger to digital data output	3 Sample clock periods + 600 ns	Maximum; Start trigger and Script triggers.

Events (Generated from the NI 6544/6545/6547/6548)

Specification	Value	Comments
Event type	1. Marker <0..2> (generation sessions only) 2. Data Active event (generation sessions only) 3. Ready for Start event 4. Ready for Advance event (acquisition sessions only) 5. End of Record event (acquisition sessions only)	—
Destinations	1. PFI 0 (SMA jack connectors) 2. PFI <1..3> (DDC connector) 3. PXI_TRIG<0..6> (PXI Express backplane)	Each event can be routed to any destination, except the Data Active event. The Data Active event can only be routed to the PFI channels.
Marker time resolution (placement)	Markers can be placed at any sample when using SDR mode. Markers must be placed at an integer multiple of two samples when using DDR mode.	—

Miscellaneous

Specification	Value	Comments
Warm-up time	15 minutes	—
On Board Clock characteristics (valid when PLL reference source is set to None)		
Frequency accuracy	±150 ppm	Typical, including temperature effects.
Aging	±5 ppm first year	Nominal.

Power

Specification	Value		Comments
	Characteristic	Maximum	
+3.3 VDC	1.75 A	1.77 A	Characteristic results are commensurate with an average user application using all data channels into high impedance load. Maximum results include worst case data pattern.
+12 VDC	2.2 A	2.3 A	
Total power	32.2 W	33.5 W	

Physical

Specification	Value	Comments
Dimensions	21.6 × 2.0 × 13.0 cm Single 3U CompactPCI Express slot; PXI Express compatible	—
Weight	18.3 oz (519 g)	—

I/O Panel Connectors

Label	Function(s)	Connector Type
CLK IN	External Sample clock, external Reference clock.	SMA jack
PFI 0	Events, triggers.	SMA jack
CLK OUT	External Sample clock, exported Reference clock.	SMA jack
Digital Data & Control (DDC)	Digital data channels, exported Sample clock, STROBE, events, triggers.	68pin VHDCI

Software

Specification	Value	Comments
Driver software	NI-HSDIO driver software 1.6 or later. NI-HSDIO allows you to configure and control the NI 6544/6545/6547/6548. NI-HSDIO provides application interfaces for many development environments. NI-HSDIO follows IVI application programming interface (API) guidelines.	—
Application software	NI-HSDIO provides programming interfaces for the following application development environments (ADEs): National Instruments LabVIEW National Instruments LabWindows™/CVI™ Microsoft Visual C/C++	See the *NI-HSDIO Instrument Driver Readme* for more information about specific versions of each ADE that are supported.
Test panel	National Instruments Measurement & Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6544/6545/6547/6548. MAX is included on the NI-HSDIO driver CD.	—

Environment

Note To ensure that the NI 6544/6545/6547/6548 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included with the NI 6544/6545/6547/6548. The NI 6544/6545/6547/6548 is intended for indoor use only.

Specification	Value	Comments
Operating temperature	0 to +55 °C in all NI PXI Express and hybrid NI PXI chassis.	—
Storage temperature	–20 to +70 °C	—
Operating relative humidity	10% to 90% relative humidity, noncondensing (Meets IEC-60068-2-56)	—

Specification	Value	Comments
Storage relative humidity	5% to 95% relative humidity, noncondensing (Meets IEC-60068-2-56)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Storage shock	50 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	—
Operating vibration	5 Hz to 500 Hz, 0.31 g_{rms} (Meets IEC 60068-2-64.)	—
Storage vibration	5 Hz to 500 Hz, 2.46 g_{rms} (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	—
Altitude	0 m to 2,000 m above sea level (at 25° C ambient temperature)	—
Pollution Degree	2	—

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:
IEC 61010-1, EN 61010-1
UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

EN 61326 (IEC 61326): Class A emissions; Basic immunity
EN 55011 (CISPR 11): Group 1, Class A emissions
AS/NZS CISPR 11: Group 1, Class A emissions
FCC 47 CFR Part 15B: Class A emissions
ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Note For EMC compliance, operate this device with the use of SHC68-C68-D4 shielded cable and provided cable ferrites. In addition, filler panels must be installed.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:
2006/95/EC; Low-Voltage Directive (safety)
2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by module number or product line, and click the appropriate link in the Certification column.

Environmental Management

National Instruments is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of their life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.

电子信息产品污染控制管理办法 （中国 RoHS）

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