# GX5296

## DYNAMIC DIGITAL I/O WITH PER CHANNEL TIMING, PROGRAMMABLE LOGIC LEVELS AND PMU PXI CARD

- Timing per pin, multiple time sets and flexible sequencer
- 32 input / output channels with PMU per pin
- 4 control / timing channels with programmable levels & PMU
- 64 Mb / channel vector memory
- Per channel drive / sense voltage range of -2 V to +7 V
- 125 MHz vector rate

## DESCRIPTION

The GX5296 offers the most performance and features of any 3U PXI dynamic digital I/O board on the market today. The 32-channel, GX5296 offers timing per pin, multiple time sets, data formatting, and an advanced sequencer – providing users with the capability emulate and test complex digital busses for system, board or device test applications. Offering 1 ns edge placement resolution per pin and a PMU per pin, the GX5296 has the ability to perform both DC and AC parametric testing. Each digital channel can be individually programmed for a drive hi, drive lo, sense hi, sense lo, and load value (with commutation voltage level). In addition, each channel offers a parametric measurement unit (PMU) providing users with the capability to perform parallel DC measurements on the DUT (device under test).

The GX5296 supports deep pattern memory by offering 64 Mb per pin of vector memory with dynamic per pin direction control and with test rates up to 125 MHz. The board supports both Stimulus / Response and Real-time Compare modes of operation, allowing the user to maximize test throughput for go / no-go testing of components and UUTs that require deep memory test patterns. The single board design supports both master and slave functionality without the use of add-on modules.

## FEATURES

The GX5296's timing generator supports 4 timing phases and windows (drive and sense timing). Each phase and window is comprised of two timing edges - assert / de-assert and an open window / close window respectively. Timing resolution of 1ns is supported for each of these edges. Four time sets are available for mapping edge timing to each channel.
Up to 64 unique time set combinations can be defined.

Additionally, six data formats are supported - NR (no return), R0, R1, RHiZ, and RC (Return to Complement), RSC (Return Surround with Complement).

Pin electronic resources are independent on a per channel basis and include a full-featured PMU for DC characterization of DUTs. The PMU can operate in the force voltage / measure current or force current / measure voltage mode. Additionally, 4 additional pin electronics resources are available for use as timing and/or control resources – providing programmable drive and sense levels from -2 to +7 volts.

The GX5296 employs a PLL based, clock system which offers programmable vector clock rates up to 125 MHz. In addition, a clocks per pattern (CPP) divider is available, providing additional clocking and edge placement flexibility. External input and output synchronization signals are also supported, providing the ability to synchronize the GX5296 to external events or time bases.

The GX5296's offers a full-featured sequencer. Capabilities include conditional jump, unconditional jump, subroutine jump, or looping (with nested loops). Additionally, the sequencer has the ability to handshake with various signals in order to synchronize with a UUT. Handshaking settings can be selected on a per Step basis where various Handshake Pause and Resume resources can be used. Total sequencer memory size is 4096 steps.

DIGITAL I/O

# GX5296

## SOFTWARE

The GX5296 is supplied with graphical vector development / waveform display tools as well as a virtual instrument panel, 32 / 64-bit DLL driver libraries, and documentation. The virtual panel can be used to interactively control and monitor the instrument from a window that displays the instrument's current settings and status. In addition, various interface files provide access to the instrument's function library for programming tools and languages such as ATEasy, C/C++, Microsoft Visual Basic®, Delphi, and LabVIEW.

## APPLICATIONS

- Semiconductor test
- ASICs testing
- A/D and D/A testing
- Video acquisition / playback applications
- High speed, bi-directional bus testing / emulation

## SPECIFICATIONS

| CHANNEL I/O SPECIFICATIONS | |
|---|---|
| Number of Data I/O Channels | 32 per card |
| Auxilary I/O Channels | 4, can be used for timing / control functions. Auxiliary channels offer all features supported by the data channels including a PMU per channel without vector memory. |
| Channel Direction Control | Input or Output per vector, per channel |
| Number of Drive and Sense Voltage References | 32 Drive Hi / Drive Lo<br>32 Sense Hi / Sense Lo |
| Drive Voltage Level | Drive Hi: -2 V to +7 V<br>Drive Lo: -2 V to +7 V<br>Maximum swing: 8 V |
| Drive Voltage Accuracy | ±15 mV (max) |
| Drive Voltage Resolution | 16 bits, 250 uV |
| Driver Leakage Current | ±15 nA (max) |
| Output Impedance | 50 Ω (typ) |
| Drive Current | ±35 mA (max) |
| Rise / Fall Times | 0.5 ns typical for a 2 V pulse |
| Channel Skew | 160 ps, typical between the same card 320 ps max, after calibration, for all channels within a domain (Drive and sense) |
| Sense Voltage Range | Sense Hi: -2 V to +7 V<br>Sense Lo: -2 V to +7 V |
| Sense Voltage Threshold Accuracy | ±15 mV |
| Sense Voltage Resolution | 16 bits, 250 uV |
| Input Leakage Current | ±15 nA (max) |
| Minimum Data Sense Pulse Width | 1.0 ns (typ) |
| Pull-Up / Pull-Down Current Source / Sink | ±24 mA, programmable on a per channel basis<br>V commutate: -2 V to +7 V, programmable on a per channel basis |
| Pull-Up / Pull-Down Current Source / Sink Accuracy | ±64 uA |
| Pull-Up / Pull-Down Current Source / Sink Resolution | 16 bits |
| Voltage Commutation Accuracy | ±15 mV |
| Voltage Commutation Resolution | 16 bits |
| Memory | 64 Mb per channel |
| Data Output Formats (per channel) | Drive Hi, Drive Lo, Hi-Z<br>Formatted Data: No return, Return to 1, Return to 0, Return to Hi-Z, Return to complement, Surround by complement; selectable on a per channel basis |
| Drive Data Timing (per channel) | Data assert / de-assert based on Phases 1-4 |
| Capture Mode (per channel) | Mask<br>Opening edge of Window<br>Closing edge of Window<br>Window – data is valid for entire window duration |
| **TEST MODES** | |
| Drive / Expect Mode | Output: Drive Hi, Drive Lo, Hi-Z<br>Expect: 1, 0, OK, between states, or mask<br>Keep last<br>Toggle last |
| Recording Modes (per sequence step) | Record errors for programmable inputs that have Good 1 & Good 0<br>Record errors for inputs that have only a Good 1<br>Record raw data based on NOT a Good 0<br>Record raw data based on a Good 1 |

# GX5296

| | |
|---|---|
| **Error Address Record** | Record address for memory errors<br>1K deep error memory |
| **TIMING** | |
| **Master Clock (PLL) Frequency Range** | 1 MHz (min); 125 MHz (max) |
| **Programming Resolution** | 5 digits |
| **Accuracy** | ±0.02% of programmed value + accuracy of reference clock (PXI 10 MHz or external reference clock) |
| **Jitter** | 50 ps RMS, typical |
| **Reference** | PXI 10 MHz clock or XClk (external clock) input |
| **Clocks per Vector Range** | Programmable, 1 to 256 |
| **Time Sets (TS0 - TS3)** | 4 phases, 4 windows;<br>user assigned to DIO channels |
| **Timing Set Sequence Control** | 64 Timing Sets with 4 Phases, 4 Windows, and 4 K sequence steps |
| **Phase and Window Timing Resolution** | 1 ns, using the 125 MHz master clock |
| **Minimum Phase / Window Pulse Width; Assert / Return Or Open / Close** | 5 ns |
| **Phase / Window Reference** | Phase: System or Pattern Clock (selectable per Seq Step)<br>Window: Pattern clock only |
| **EXTERNAL STATUS AND CONTROL SIGNALS** | |
| **Logic Levels** | LVTTL or programmable level using one of the four Aux pin electronics channels. |
| **Trigger Source** | Software, PXI trigger bus, External event, External trigger input |
| **Sync Outputs** | Start of Sequence; Start of Sequence Step |
| **Input Aux I/O Selections** | Synthesizer reference clock, System clock, Break (System Clutch), Halt (Pattern Clutch), Sequence Jump signals |
| **Output Aux I/O Selections** | Phase, Window, Waveform, Syncs, Seqflag, Seq Active, Seq Idle, T0_Clk , Pat_Clk, |
| **SEQUENCER** | |
| **Commands** | Jump, Conditional Jump, Loop, Call Subroutine, Return, Pause, Halt |
| **Loop Counters** | 16, can be nested<br>Only one can end on a sequence step<br>Loop count range: 1 – 64K or continuous |

| | |
|---|---|
| **Test Inputs** | External: PXI triggers, Aux I/O<br>Internal: Data sense, Edge or level |
| **Sequencer Memory** | 4096 Steps |
| **Phase Trigger** | T0_CLK or PAT_CLK |
| **Window Trigger** | PAT_CLK |
| **Patterns per Sequence Step** | 1 to 64M |
| **Sequence Loop** | 1 to 1M, continuous |
| **Current Step Loop** | 1-65535, continuous |
| **Multi Step Loop** | 1-65535, nested 16 deep |
| **Jump** | Conditional / Unconditional |
| **Jump Conditions** | Error True, Sequence Timeout True, Signal Level (High / Low), Signal Edge (Rising / Falling) |

| **PARAMETRIC MEASUREMENT (PMU)** | |
|---|---|
| **Number of Parametric Measurement Units** | 32, one per channel<br>4, one per auxiliary channel (for timing /control & static I/O functions) |
| **Configurations** | Force Voltage/Measure Current (FVMI)<br>Force Current/Measure Voltage (FIMV)<br>Force Voltage/Measure Voltage (FVMV)<br>Force Current/Measure Current (FIMI) |
| **Force Voltage Range** | -1.5 V to +7 V |
| **Force Voltage Accuracy** | ±15 mV |
| **Force Voltage Resolution** | 16 bits |
| **Force Current Ranges** | ±32 mA, ±8 mA, ±2 mA, ±512 uA, ±128 uA, ±32 uA, ±8 uA, ±2 uA FS |
| **Force Current Accuracy; Compliance Range:**<br>**+7 V to +1.75 V @ 32 mA,**<br>**+7 V to -1.5 V @ no load** | ±120 uA, 32 mA range<br>±40 uA, 8 mA range<br>±5uA, 2 mA range<br>±1.2 uA, 512 uA range<br>±600 nA, 128 uA range<br>±160 nA, 32 uA range<br>±80 nA, 8 uA range<br>±20 nA, 2 uA range |

# GX5296

| | |
|---|---|
| **Current Measurement Accuracy (60 Measurements / Sec); Compliance Range: +7 V to +1.75 V @ 32 mA +7 V to -1.5 V @ no load** | ±120 uA, 32 mA range<br>±40 uA, 8 mA range<br>±5 uA, 2 mA range<br>±1.2 uA, 512 uA range<br>±600 nA, 128 uA range<br>±160 nA, 32 uA range<br>±80 nA, 8 uA range<br>±20 nA, 2 uA range |
| **Measure Voltage Range** | -2 V to +7 V |
| **Measure Voltage Accuracy** | ±1 mV (measurement rate < 200 measurements / sec) |
| **High and Low Commutation Voltage Range** | VCLo: -2 V to +5 V<br>VCHi: 0 V to +7 V |
| **Voltage Clamp Accuracy** | ±100 mV |
| **POWER (IDLE AND INITIALIZED)** | |
| **+3.3 $V_{DC}$** | 4.8 A |
| **+5 $V_{DC}$** | 1.48 A |
| **+12 $V_{DC}$** | 0.25 A |

| | |
|---|---|
| **ENVIRONMENTAL** | |
| **Operating Temperature** | 0 °C to +50 °C |
| **Storage Temperature** | -20 °C to +70 °C |
| **Size** | 3U PXI |
| **Weight** | 200 g |
| **FRONT PANEL CONNECTORS** | |
| **J1** | Digital I/O Signals, type 68-pin VHD connector |
| **J3** | Timing & Control Signals, type 68-pin VHD connector |

Note: Specifications are subject to change without notice

## ORDERING INFORMATION

| | |
|---|---|
| **GX5296** | Dynamic Digital I/O (3U), 32 ch., per pin voltage & direction control; 125 MHz w/256 MB memory; per pin timing & PMU |
| **SOFTWARE** | |
| **GtDio6x-FIT** | File import tool for importing and converting STIL, WGL, VCD/EVCD, ATP vectors |
| **ACCESSORY** | |

| | |
|---|---|
| **GT95014** | Connector Interface for GT5xxx/GX5xxx/GC5xxx, SCSI to 100 Mil Grid, Single Ended |
| **GT95021** | 2' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95022** | 3' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95022E** | 3' shielded cable for 5xxx/35xx products (68 Pin) not terminated one end |
| **GT95025** | Connector Interface, 68-Pin SCSI to TTI Testron 170-Pin Signal Block |
| **GT95028** | 10' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95031** | 6' shielded cable for 5xxx/35xx products (68 Pin) |
| **GT95032** | 6" Shielded Cable for all 5xxx/35xx (68 Pin) |
| **GT95032-8** | 8" Shielded Cable for all 5xxx/35xx (68 Pin) |
| **GT95032-12** | 12" Shielded Cable for all 5xxx/35xx (68 Pin) |