GX5291 SERIES

3U PXI HIGH SPEED DYNAMIC DIGITAL I/O CARD

- Cost effective, performance digital solution for low pin count applications
- 32 input / output channels, dynamically configurable on a per channel basis
- 128 MB of on-board vector memory
- Supports 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V TTL/LVTTL logic familes
- 50 or 100 MHz vector rate versions

DIGITAL I/O

DESCRIPTION

The GX5291 is a high performance, cost-effective 3U PXI dynamic digital I/O boards offering 32 TTL or LVDS input or output channels with dynamic direction control. The GX5291 also supports deep pattern memory by offering 128 MB of on-board vector memory with dynamic per pin direction control and with test rates up to 100 MHz.

FEATURES

The GX5291 supports selectable I/O levels of 1.5 V, 1.8 V, 2.5 V, or 3.3 V (TTL, LVTTL, CMOS, LVCMOS). The TTL/LVTTL interface utilizes a programmable voltage source, which sets the output logic levels from 1.4 V to 3.6 V. Programmable thresholds of 1.5V, 1.8V, 2.5V or 3.3V (5V compatible) supports standard logic input signals. Recommended operating input voltage range is from 0 V to 5.5 V.

A windowing method is utilized for PCI memory accesses, which limits the required PCI memory space for each board to only 16MB, thus preserving test system resources. A direct mode, for continuous data transfer between the test system controller and the I/O pins of the GX5291 is also supported.

The GX5291 offers 128 MB of vector memory, with 32 Mb per channel. Programmable I/O width allows trading vector width for vector depth. Under software control, the GX5291's vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 with corresponding vector depths of 32 Mb, 64 Mb, 128 Mb, 256 Mb, 512 Mb, and 1024 Mb.
The GX5291 provides programmable TTL/LVTTL output clocks and strobes, and supports external clock and strobe. A programmable PLL (phase locked loop) provides configurable clock frequencies and delays.

The GX5291's sequencer can halt or pause on a defined address or loop through the entire memory as well as loop on a defined address range or through a defined block of memory.

SOFTWARE

The GX5291 is supplied with DIOEasy, which provides powerful graphical vector development / waveform display tools as well as a virtual instrument panel, 32-bit DLL driver libraries, and documentation. The virtual panel can be used to interactively adjust and control the instrument from a window that displays the instrument's current settings and status. In addition, various interface files provide access to the library for programming tools and languages such as ATEasy, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, and LabVIEW.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Displays, printers, and disk drive testing
- ASICs testing
- A/D and D/A testing
- Video acquisition / playback applications
- High speed, bi-directional bus testing / emulation

Geotest Marvin Test Systems,Inc.
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GX5291 SERIES

SPECIFICATIONS

INPUT / OUPUT CHANNEL FEATURES	
DATA DIRECTION CONTROL	Dynamically controlled on a per vector and per channel basis
CHANNELS PER BOARD	32
CHANNEL CONFIGURATION PER BOARD (SOFTWARE CONTROLLED)	32 / 16 / 8 / 4 / 2 / 1
LOGIC FAMILIES	TTL/LVTTL/CMOS/LVCMOS (1.5 V, 1.8 V, 2.5 V, 3.3 V, or 5 V compatible)
I/O LEVELS	TTL/LVTTL/CMOS/LVCMOS: Programmable Output Voltage Level 1.4 V (Min); 3.6 V (Max) Input Threshold (selectable) 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant) Supports standard logic levels Recommended Operating Conditions 0V (Min); 5.5V (Max)
MEMORY DEPTH PER CHANNEL	32 Mb - 1Gb, programmable
CHANNEL TIMING SKEW	+/- 1 nS
TIMING	
INTERNAL TEST CLOCK (PLL)	
FREQUENCY RANGE	5 Hz (Min.); 100 MHz (Max.), GX5291-100 50 MHz (Max.), GX5291-50
ACCURACY	Greater of (+/- 1Hz or +/- 0.02% of programmed value) + accuracy of reference clock (PXI 10 MHz or external reference clock)
JITTER	+/- 20 mUI of internal clock frequency, max
REFERENCE	PXI 10 MHz clock or XClk (external clock) input
INTERNAL B CLOCK OUTPUT (TTL/LVTTL)	
FREQUENCY RANGE	300 KHz (Min.); 100 MHz (Max.), GX5291-100 50 MHz (Max), GX5291-50
ACCURACY	Greater of (+/- 1 Hz or +/- 0.5% of programmed value) + accuracy of the reference clock
INTERNAL STROBE (OSTB) AND OUTPUT CLOCK (OCLK) OUTPUTS, CLOCK AND DATA TIMING	
LOGIC LEVELS	TTL / LVTTL / CMOS / LVCMOS, programmable output voltage level, 1.4 V (min) to 3.6 V (max)
FREQUENCY	Internal clock or External strobe, External clock inputs
PROGRAMMABLE DELAYS (USING INTERNAL CLOCK SOURCE ONLY) FOR INTERNAL STROBE AND OUTPUT CLOCK SIGNALS	0 – 27nS in 250pS steps (5 Hz to 100 MHz), GX5291-100 0 – 27nS in 250pS steps (5 Hz to 50 MHz),, GX5292-50
OUTPUT CLOCK TO DATA OUTPUT DELAY	__nS, active OCLK clock edge to valid data
STROBE CLOCK TO DATA INPUT	__nS data setup time (min) __nS data hold time (min) Relative to OSTB clock edge

EXTERNAL TEST CLOCK INPUT	
FREQUENCY RANGE (CONFIGURED AS SAMPLE CLOCK)	0 Hz (Min.); 100 MHz (Max.), GX5291-100 0 Hz (Min.); 50 MHz (Max.),, GX5291-50
FREQUENCY RANGE (CONFIGURED AS REFERENCE CLOCK TO PLL)	8MHz to 10.5 MHz
PULSE WIDTH	40% Min, 60% Max
INPUT LOGIC LEVELS	User selectable I/O level, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, (5 V tolerant), TTL, / LVTTL / CMOS, / LVCMOS
EXTERNAL STROBE CLOCK INPUT	
FREQUENCY RANGE	0 to 100MHz , GX5291-100 0 to 50 MHz, GX5291-50
LOGIC LEVELS	TTL / LVTTL / CMOS / LVCMOS Input threshold: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5V tolerant)
EXTERNAL STATUS & CONTROL SIGNALS	
LOGIC LEVELS	TTL/LVTTL/CMOS/LVCMOS: Prog. Output Voltage Level: 1.4 V (Min); 3.6 V (Max) Input Threshold: 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant)
TRIGGER SOURCE	Software, PXI trigger bus, External event, External trigger input (overrides Run command)
EXTERNAL CLOCK ENABLE	Internal (software) or External input (via J3 connector)
EXTERNAL STROBE ENABLE	Internal (software) or External input (via J3 connector)
EXTERNAL EVENT BUS	16 input lines with mask and logic AND conditioning
PAUSE	External pause input overrides Pause command
PAUSE LATENCY	10 clock cycles to acquire data after pause deasserts
RUN	Run status indicator (J3 connector)
POWER	
3.3 VDC	200 mA (Min.); 4 A (Max.)
5 VDC	50 mA (Min.); 2 A (Max.)
12 VDC	0.03mA (Min.); 0.1mA (Max.)
FRONT PANEL CONNECTORS	
J1	I/O TTL Signals, 68-pin VHD connector
J3	Timing / Status Signals, 68-pin VHD connector
J4	Control Signals, 68-pin VHD connector
ENVIRONMENTAL	
OPERATING TEMPERATURE	0 to 50° C
STORAGE TEMPERATURE	-20° C to 70° C
SIZE	3U PXI
WEIGHT	200 g
Note: Specifications are subject to change without notice.	

ORDERING INFORMATION

GX5291-100	100 MHz Digital I/O Board with 128 MB of vector memory
GX5291-50	50 MHz Digital I/O Board with 128 MB of vector memory
ACCESSORIES	
GT95014	Connector interface, SCSI to 100 Mil Grid, Single Ended I/F Board
GT95015	Connector Interface for all 5xxx/35xx, SCSI to 100 Mil Grid, differential
GT95021	2' shielded cable (68-pin SCSI)
GT95022	3' Shielded cable (68-pin SCSI)
GT95028	10' Shielded cable (68-pin SCSI)
GT95031	6' Shielded cable (68-pin SCSI)

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