

# Fastbit

## FB100A BER Test System



**AEROFLEX**  
A passion for performance.

Highly flexible BER test system for serial and parallel testing over a wide range of interfaces from TTL to optical. Addresses system, sub-system and component testing during development and compliance verification in IC, cable, satellite, cellular, terrestrial, CATV, digital TV and other physical layer test markets. Extensive options for accurate, comprehensive generation of RF channel impairments for the testing of RF communications systems and equipment.

- Windows NT user interface
- Up to 160 Mbit/s operation
- Resident interfaces for TTL, ECL and PECL
- Interface Pods for TTL, LVDS, RS-422 (V.11), MPEG SPI, ASI, OC3 and HSSI
- Signal connection capability includes "Pod to Header" and a "Pod to Micro-grabbers" for circuit card and device probing
- Telecom Data Interface Pod for X.21, RS-449, V.35, V.36, RS-232 and EIA/TIA530/A interfaces
- Serial and 8 bit wide parallel data on TTL Pod
- 8 bit wide parallel data on LVDS and RS-422 (V.11) Pods
- Broadband Impairment Generation Options
  - Frequency tunable noise from 5 MHz to 2.4 GHz with selectable channel bandwidths
  - High accuracy, wide dynamic range Carrier to Noise and Interference
  - Selectable Burst Noise and Flat Fading carrier profiles
  - Automatic BER versus Carrier to Noise

### Broadband Physical Layer Transmission Test Issues

As demand grows for high-speed video, audio and data transmission, so grows the job of today's communications engineer. More bits through

limited bandwidth in a noisy channel means using creative engineering to guarantee fast, error-free data transmission. Unfortunately, data transmission test equipment hasn't kept pace with technology. Design engineers are having to spend valuable time developing custom interfaces to connect test equipment to their device under test. Parallel high speed data interfaces into the modulator and out of the demodulator are becoming more common than the older serial interfaces. To connect easily, test equipment needs to support these interfaces. Typically, auxiliary signaling is needed to accompany clock and data during testing to control data flow and flag valid data frames. These additional signals were not designed into traditional bit error rate testers in use today. Frustrations also arise with test data formatting. Because error correction schemes are in use, data is sent in transport frames with header and error correction bytes. To be useful, modern day data generators and error analyzers must provide more than simple pseudo-random test sequences. Lastly, valuable development time is lost coding custom test software to control BERT, modulator and channel impairment equipment from different test equipment vendors. Custom interface circuitry and software is expensive to develop, document and support, be it in the lab, or out at a customer site.

The FB100A is a modular, expandable, high data rate bit error test system. This system was developed with the R&D and test engineer in mind to allow quick and easy characterization of broadband PHY device BER performance.

### Flexible Serial and Parallel I/O

The FB100A is designed to plug in and connect to almost any modulator, evaluation board or set-top box. This is because the data generator and error detector both offer serial and parallel interfaces. All interfaces support a multitude of selectable logic levels. Clock and data signals are complemented with supplemental I/O to simulate your specific handshaking requirements.

For the very latest specifications visit [www.aeroflex.com](http://www.aeroflex.com)

## Comprehensive Pattern Generation and Error Analysis

User programmable pattern generation, as well as supplemental I/O, provide immediate connectivity to the device under test (DUT). The FB100A pattern generator allows the user to construct overhead and payload test frames specific to almost any standard. In addition, the data analyzer's INSTALOK™ two-step "SYNC" process deciphers framing and payload, and synchronizes immediately to the incoming data stream ideal for testing DVB, MCNS, DSS, and xDSL compliant electronics.

## BROADBAND IMPAIRMENT GENERATION PROBLEMS AND SOLUTIONS

RF communication technology in the CATV, satellite, DTV, MDS, and wireless market spaces has driven the need for accurate, comprehensive generation of RF channel impairments, such as noise and interference.

For a fuller description see the Fast Bit FB2000A data sheet.

## NOISE AND RF INTERFERENCE GENERATION

### Carrier to Noise PLUS Interference

Simulation of real-world conditions in the lab requires simultaneous level setting and summing of in-band and out-of-band impairments and accurately ratioed carrier and noise. The frequency tunable noise source option enables noise addition in five user-selectable bandwidths at any frequency from 5 MHz to 2.4 GHz. In addition up to four external interferer signals can be added anywhere in the 5 MHz to 2.4 GHz spectrum and ratioed to the carrier with 0.1 dB resolution and 0.1 dB typical accuracy, thus supporting co-channel, adjacent channel and total interferer power test requirements. Industry standard conformance tests for BER can be run from this instrument without the use of external RF attenuators, combiners or additional test fixtures.

### High Accuracy, Wide Range Eb/No, Over Large Carrier Dynamic Range

There is ample noise power to set low carrier to noise ratios at high carrier levels and noise bandwidth matching enables high inband noise densities without overloading the test device's front end. In contrast, high carrier to noise ratios at carrier power levels as low as -70 dBm are possible, while maintaining the instrument's intrinsic accuracy.

### Burst Noise

Burst noise can be generated for testing the performance of demodulators used for cable and digital TV transmission. Options are available for both internal and external programming of the burst noise parameters.

### Carrier And Interferer Flat Fading

A receiver's AGC can be tested using the Flat Fading option. The user can program the C/N ratio, and the carrier fading depth and period using sinusoidal or triangle wave profiles, while keeping the noise level fixed. Alternatively, interferer or noise signal levels can be varied using the same approach, while keeping the carrier level fixed.

## AUTOMATED BER MEASUREMENTS

Optional BER calculator software enables automatic BER measurements over a range of carrier to noise ratios. Software includes theo-

retical curves for performance comparisons, and test time can be optimized against required accuracy and confidence levels. Dramatic improvements in accuracy and test time are achieved compared to other methods.

## Based on WINDOWS NT Technology

By using PC technology, the FB100A is capable of expanding with your needs. Look to Fast Bit Technologies to provide "future-proof", turnkey PHY testing.

## SPECIFICATION

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### DATA GENERATOR

100 bit/s - 160 Mbit/s (From 0 Hz with external clock)

### OPERATING BIT RATE RANGES

#### Serial

100 bit/s - 50 Mbit/s (100Mbit/s with FB100 OP6 option) (From 0 Hz with external clock)

#### Parallel 8

800 bit/s - 20 Mbit/s (160 Mbit/s with FB100 OP6 option) (From 0 Hz with external clock)

### INTERNAL CLOCK SOURCE

100 Hz - 100 MHz

1 Hz resolution

### PATTERNS

#### PRBS Codes

2<sup>7</sup>-1, 2<sup>11</sup>-1, 2<sup>15</sup>-1, 2<sup>20</sup>-1, 2<sup>23</sup>-1

#### WORD

4 Mbit user defined

#### FRAMED PRBS/WORD

4 Mbit user defined

#### SYNC1 PATTERN

4 Mbit user defined

Independent PRBS, Word and per Channel Data Invert

### GENERATOR INPUTS

External Clock input - 0 Hz to 100 MHz

External 10 MHz Reference input

External Clock disable input

### GENERATOR OUTPUTS

#### Serial

Data, Data Invert, Clock, Clock Invert, Sync1, Sync2 (or Sync1 Invert)

TTL or differential PECL, selectable

#### Parallel 8 (via optional PODs)

Serial/parallel TTL

LVDS (MPEG2P - SPI)

RS-422 (MPEG2P)

ASI

HSSI

OC3/SONET/SDH - 155 Mbit/s

Telecom Data Interface  
RS-232, EIA/TIA 530/A, RS-449 (V.36), X.21, V.35

#### **Clock and Sync**

Scope Sync output  
Clock Source output (full rate clock)  
10 MHz Clock Reference output

#### **GENERATOR ERROR INJECT**

Single  
Rates:  $1 \times 10^N$ ,  $N = 2, 3, 4, 5, 6, 7, 8, 9$

#### **ANALYZER INPUTS**

##### **Serial**

Data, Data Invert, Clock, Clock Invert, Sync3, Sync4, DFAIL (default: Sync3 is PSYNC, Sync4 is DVALID)

Differential or Internal Threshold for Single Ended Inputs

Threshold range -4.0 V to +5.0 V for clock and data

Selectable termination 50 ohms to +3 V, +1.5 V, GND, or -2 V

##### **Parallel 8 (via optional PODs)**

Serial/parallel TTL  
LVDS (MPEG2P - SPI)  
RS-422 (MPEG2P)  
ASI  
HSSI  
OC3/SONET/SDH - 155 Mbit/s  
Telecom Data Interface  
RS-232, EIA/TIA 530/A, RS-449 (V.36), X.21, V.35

#### **ANALYZER SYNCHRONIZATION**

PRBS using feed forward  
WORD using Frame Sync Word or Selectable threshold  
Mixed (WORD/PRBS)  
Frame Sync Word and PRBS feed forward  
PSYNC (Frame Sync Marker) and PRBS feed forward

#### **FRAME SYNC WORD**

Length selectable from first 8, 16 or 24 bits of Word Pattern  
Programmable consecutive number of frames to Acquire/Lose Sync is 1 to 15.

#### **ANALYZER CLOCK/DATA DE-SKEW**

##### **Serial**

Clock delay 0-15 ns  
Clock Invert

##### **Parallel**

Clock delay 0-15 ns  
Clock Invert

#### **ERROR COUNTS/RATES**

Bit  
Word (8 bit)  
Block (Programmable 16 bits - 4 Mbit)  
Bit Errors per channel

Frame Errors (Using PSYNC and DFAIL)

#### **MEASUREMENT MODES**

Total - Error Data since start of test  
1 second - Current Error Data in last 1 second  
Window - Error Data in sliding 10 second window

#### **ANALYZER PARALLEL PACKET FILTER**

Uses 2nd and 3rd bytes of Packet for packet identification

#### **ANALYZER STATUS INDICATORS**

In SYNC  
PRBS Sync LOSS  
Word Sync LOSS  
Frame Sync LOSS  
Data Loss  
Clock Loss  
Bit ERRORS (per channel)  
DFAIL error  
Internal Clock OOL (out of lock)  
Bit Rate  
Test Running

#### **COMMUNICATIONS INTERFACES**

RS232C (2)  
IEEE488.2  
PARALLEL

#### **PHYSICAL**

##### **Weight**

18 kg (40 lbs)

##### **Size**

Height	Width	Depth
210 mm	410 mm	510 mm
8"	6"	20"

#### **NOISE AND INTERFERENCE GENERATION OPTIONS**

See FB2000A Datasheet

#### **VERSIONS AND ACCESSORIES**

When ordering please quote the full ordering number information.

##### **Ordering Numbers**

FB100A

##### **Versions**

Base Unit, Serial BER Test System 50 Mbit/s

PECL/TTL serial I/O interface only

Includes Performance Verification Package - six (6) 50 Ohm BNC RG58C/U Cables, 0.3 m (1') and one (1) Parallel DB50 to DB50 Cable, 1.8 m (6') (FBACC107)

No parallel interface included

## Options and Accessories

FB100 OP1	ECL replacing PECL. PECL is Standard.
FB100 ACC2B	Parallel LVDS interface Pods (MPEG2P option)
FB100 ACC2C	Parallel RS-422 (V.11) interface Pods (DVB-SPI compatible, MPEG2P option)
FB100 ACC2D	ASI Interface Pod
FB100 ACC2H	Serial/Parallel TTL interface Pods

\* Parallel BER and Parallel I/O Port are included if any pods are ordered with the FB100A. Additional Pods can be added as required.

FB100 ACC2J	OC3/STM-1 rate transceiver interface Pods. Specify ST, FC or SC receptacle. Must have OP6.
FB100 ACC2K	Telecom Data Interface Pod - Synchronous and Asynchronous (Transmit and receive).

### Optional Cable Assemblies

FBACC106	RS-232, EIA/TIA530/A
FBACC108	X.21
FBACC109	V.35
FBACC110	RS-449 (V.36)
FB100 ACC2L	HSSI Pod (Transmit and Receive) High Speed Serial Interface (ECL logic, byte-wide data)
FB100 OP6	Increased Speed/High Data Rate Bert (Serial: 100 Mbit/s, Parallel: 160 Mbit/s). Must be ordered for parallel interfacing.
FB100 OP7	BER Pre-Calculator Software, BER vs. Eb/No graphing. Must have OP210 or OP215.
FB100 OP206	IEEE-448 (GPIB)
FB100 OP210	Frequency Tunable Carrier to Noise Module (5 MHz - 1.0 GHz)
FB100 OP215	Frequency Tunable Carrier to Noise Module (5 MHz - 2.4 GHz)
FB100 OP220	200 MHz Bandwidth Filter for C/N; replaces the standard 100 MHz filter. Must have OP210 or OP215 installed.

FB100 OP220A	500 MHz Bandwidth Filter for C/N; replaces the standard 100 MHz filter. Must have OP210 or OP215 installed.
FB100 OP225	C/I internal ratio setting for two external impairments. Must have OP210 or OP215 installed.
FB100 OP225B	Additional two inputs for C/I ratio external impairments. (Total of 4 inputs - 2 summed pairs). Must have OP225 installed.
FB100 OP226	75 Ohm BNC connectors on the interferer inputs. The interferer input is 50 ohm standard.
FB100 OP229	Internal Burst Noise. Must have OP210 or OP215.
FB100 OP229B †	External Burst Noise. Must have OP210 or OP215.
FB100 OP230 †	Broadband Noise Loading. Used to simulate RF front end.
FB100 OP240	Cellular Low Power Option. For power low as -140 dBm. Either OP240 or OP240B may be installed, not both.
FB100 OP240B	Large negative SNR settings option. Allows the setting of large, negative C/N, C/I ratios. Either OP240B or OP240 may be installed, not both.
FB100 OP248	Flat Fading. Interferer, Carrier and Noise flat fading
FB100 OP249 †	TDMA. Allows C/N and C/I setting on burst signals and allows C/N or C/I setting on a TDMA signal.
FB100 OP905	Touch Screen
WARRANTY	Two years

† Only two of these three options can be fitted.

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